CBCS SCHEME

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15EC751

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Define LTI system. **(04 Marks)**

b. Evaluate in detail decimation and interpolation process with neat block diagram and necessary equations. **(06 Marks)**

c. Determine the interpolated sequence y(m) with input sequence x(n) = [0, 3, 6, 9] using interpolation sequence $b_k = \left[\frac{1}{3}, \frac{2}{3}, \frac{3}{3}, \frac{2}{3}, \frac{1}{3}\right]$ and interpolation factor of 3. **(06 Marks)**

OR

2 a. Define Dynamic range and resolution. **(04 Marks)**

b. Interpret the D/A converter error due to zero order hold at its output. **(06 Marks)**

c. Calculate the Dynamic range and percentage resolution of each of the following number representation formats.
   i) 24-bit, single precision, fixed point format.
   ii) 48-bit, double precision fixed point format
   iii) A floating point format with a 16-bit mantissa and an 8-bit exponent. **(06 Marks)**

Module-2

3 a. What is Barrel shifter? **(04 Marks)**

b. Build 4×4 Barman multiplier. **(06 Marks)**

c. Analyze circular addressing mode algorithm. **(06 Marks)**

OR

4 a. Analyze MAC unit. **(04 Marks)**

b. Elaborate the importance of saturation logic and Guard bits used in MAC unit. **(06 Marks)**

c. Analyze the importance of parallelism and pipelining used in programmable DSP with the help of 8-tap FIR Filter. **(06 Marks)**

Module-3

5 a. Distinguish the architectural features of three fixed point DSPs. **(08 Marks)**

b. Sketch the functional diagram of ALU of TMS320C54XX DSP and briefly explain. **(08 Marks)**

OR

6 a. Describe the operation of Hardware timer with a neat diagram. **(08 Marks)**

b. Write an ALP of TMS320C54XX processor to compute the sum of three product terms given by an equation.
$y(n) = h_0\, x(n) + h_1\, x(n-1) + h_2\, x(n-2)$ using MAC instruction. **(08 Marks)**

Module-4

7 a. Implement the block diagram of FIR Filter and briefly explain. **(04 Marks)**

b. Sketch the block diagram for second order IIR Filter and briefly explain. **(04 Marks)**

c. Write a program to multiply two Q15 numbers. **(08 Marks)**

OR

8 a. Derive the equations to implement a butterfly structure in DITFFT algorithm. **(04 Marks)**

b. Write the subroutine for bit reversed order. **(04 Marks)**

c. Develop the subroutine to implement butterfly computation. **(08 Marks)**

Module-5

9 a. Describe DMA with respect to TMS320C54XX processor. **(08 Marks)**

b. Interface data memory system with the address range 000800H000FFFH for TMS320C5416 processor. Use 2K×8 SRAM memory chips. **(08 Marks)**

OR

10 a. With a neat block diagram, explain the synchronous serial interface between TMS320C54XX and CoDEC device. **(08 Marks)**

b. Explain the DSP based biotelemetry Receiver system with a neat block diagram. **(08 Marks)**

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