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10EC751

Seventh Semester B.E. Degree Examination, June/July 2019
DSP Algorithm and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List and explain the commonly found unique architectural features implemental in programmable DSP devices. **(04 Marks)**

b. A simple FIR filter where output is the average of the current input x[n] and the past input x[n – 1] and given by ;
y[n] = 0.5 x[n] + 0.5 x[n – 1]
Draw the block diagram for the above equation. Find unit impulse, frequency response, magnitude response, and phase response of this filter. Also find the group delay and sketch magnitude and phase response curves. **(10 Marks)**

c. Explain with block diagram and equation the DSP operations ;
i) Decimation ii) Interpolation. **(06 Marks)**

2 a. Investigate the basic features that should be provided in the DSP architecture to be used implement the following N^{th} order FIR filter :

$$y[n] = \sum_{i=0}^{N-1} h[i]x[n-i] \quad n = 0, 1, 2, \ldots\ldots$$

Where x[n] denotes the input sample ; y[n] the output sample ; and h[i]the i^{th} filter coefficient x[n – i] is the input sample i samples earlier than x[n]. **(08 Marks)**

b. Explain circular addressing mode used in DSP device with algorithm and an example. **(08 Marks)**

c. It is required to find the sum of 64 numbers each represented by 16-bits. How many bits should the accumulator have so that the sum can be computed without the occurrence of overflow error? If accumulator is only of 16-bits, how many bits should each number be shifted before the addition to prevent overflow? What is the actual sum of number, if all numbers are fixed-point integers? What is the error in the computation of sum? **(04 Marks)**

3 a. Explain with example, the following addressing modes of TMS320C54XX processors :
i) Immediate addressing ii) Absolute addressing
iii) Accumulator addressing iv) Memory – mapped register addressing. **(08 Marks)**

b. If the contents of AR3, BK and ARO are 1040h, 45h and 0050h respectively, then find starting and ending address for the buffer when AR3 is selected as the pointer for the circular buffer. Also find the content of register AR3 after the execution of the following instructions :
i) *AR3 + 0 ii) *+ AR3(– 40h) iii) *AR3 + 0B iv) LD*AR3 + 0%, A. **(06 Marks)**

c. Explain program control unit of TMS320C54XX processors. **(06 Marks)**

4 a. Explain the following instructions of TMS320C54XX processor with examples :
i) MPY ii) MAC iii) MAS iv) RPT. **(08 Marks)**

b. Write a program using TMS320C54XX processors instruction set to compute the sum of three product terms given by the equation.
$y[n] = h_0 x[n] + h_1 x[n-1] + h_2 x[n-2]$
where x[n], x[n – 1] and x[n – 2] are data samples stored at three successive date memory locations and h_0, h_1 and h_2 are constants stored at three other successive locations in the data memory. The result y[n] is to be stored in the data memory. Use direct addressing made to access the data memory. **(06 Marks)**

c. With a neat diagram explain hardware timer circuit of TMS320C54XX processors. **(06 Marks)**

PART – B

5 a. Explain Q-notations technique used in DSP algorithm implementation. **(04 Marks)**

b. What values are represented by the 16-bit fixed point number N = 3333h in the Q_{15}, Q_8, Q_5, and Q_1 notations. **(04 Marks)**

c. With the help of block diagram, explain the implementation of an IIR filter in TMS320C54XX processors. **(06 Marks)**

d. Write a set of instructions to implement FIR filter in TMS320C54XX processors. **(06 Marks)**

6 a. Explain, how scaling present overflow conditions in the butterfly computation. **(06 Marks)**

b. Determine the following for a 128 point FFT computation :
i) Number of stages
ii) Number of butterflies in each stage
iii) Number of butterflies needed for the entire computation
iv) Number of butterflies that need no twiddle factors
v) Number of butterflies that require real twiddle factors
vi) Number of butterflies that require real complex twiddle factors. **(06 Marks)**

c. With an 8-point FFT implement structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processor using ¼ as a scaling factor for all butterflies. **(08 Marks)**

7 a. With timing diagram, explain read – write operation of memory interface signals. **(06 Marks)**

b. Design a data memory system with address range 000800h-000FFFh for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

c. Classify the interrupts and explain the interrupt handling sequence by the C54XX processors with a flow chart. **(08 Marks)**

8 a. Explain in detail with timing diagrams the synchronous serial interface of C54XX DSP. **(10 Marks)**

b. Explain DSP – based bio-telemetry receiver system with block diagram. Also explain the PPM (Pulse Position Modulation) encoding and decoding scheme used in biotelemetry receiver system. **(10 Marks)**

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