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10EC751

Seventh Semester B.E. Degree Examination, June/July 2016
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. An analog signal is sampled at the rate of 8 KHz, if 512 samples of the signal are used to compute DFT, X(k), determine the analog and digital frequency spacing between adjacent X(k) elements. Also determent analog and digital frequencies corresponding to k = 64. **(06 Marks)**

b. List the major architectural features used in DSP system to achieve high speed program execution. **(06 Marks)**

c. Explain the decimation and interpolation with equation. Let x(n) = [3, 2, –2, 0, 7]. It is interpolated using an interpolation filter b_k = [0.5, 1, 0.5] with interpolation factor–2. Determine the interpolation sequence. **(08 Marks)**

2 a. With a neat block diagram explain about the saturation logic and its use. **(06 Marks)**

b. Briefly explain about the 4 × 4 Braun multiplier with its structure. In n × n parallel multiplier structure how many adders are required? **(08 Marks)**

c. With a neat block diagram, explain address generation unit of DSP system. **(06 Marks)**

3 a. Compare architectural features of TMS320C25 and motarala fixed point DSP devices. **(06 Marks)**

b. Describe the multiplice/address unit of TMS320C54XX processor with a neat block diagram. **(06 Marks)**

c. Consider that AR3 is selected as the pointer for the circular buffer. The various register contents are B_k = 40, AR3 = 1020H, AR0 = 0025H. Find : i) start and end address of the buffer ii) contents of AR3 after the execution of the instruction LD *+AR3(12H)% iii) contents of AR3 after the instruction LD * AR3 + 0%. **(08 Marks)**

4 a. Explain the operation of serial input/outputs ports and hard ware timer of TMS320C54XX on chip peripherals. **(08 Marks)**

b. Differentiate between MAC and MACD instruction by way of explaining them. **(04 Marks)**

c. By means of a figure, show the pipeline operation of the following sequence of TMS320C54XX instruction. Assume initial value of AR3 is 80h and the values. stored in memory locations 80h, 81h, 82h as 1, 2 and 3

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LD * AR3+ , A
ADD # 1000h, A
STL A, * AR3 +.
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(08 Marks)

PART – B

5 a. What do you mean by Q–notations used in DSP algorithm implementation? What are the values represented by 16 bit numbers N = 4000h, in Q_{15}, Q_7 and Q_0 notations? **(08 Marks)**

b. Write an assembly language program for TMS32054XX processor to multiply two Q_{15} numbers to produce Q_{15} result. **(05 Marks)**

c. With the help of a block diagram, explain the implementation of an FIR filter in TMS320C54XX processor. Show the memory organization for the filter implementation. **(07 Marks)**

6 a. Why zero padding is done before computing the DFT? **(02 Marks)**

b. Explain an 8-point DIT-DFT implementation structure based on the butterfly on the TMS320C54XX. **(08 Marks)**

c. Determine optimum scaling factor to prevent over flow. **(10 Marks)**

7 a. Draw the I/o interface timing diagram for read–write–read sequence of operation. **(06 Marks)**

b. Design an interface to connect a 64k×16 flash memory to a TMS320C54XX device. The processor address bus is A_0 to A_{15}. **(06 Marks)**

c. What are interrupts? How interrupts are handled by the C54XX DSP processor? **(08 Marks)**

8 a. Explain with a neat diagram, the synchronous serial interface between the C54XX and a CODEC device, **(06 Marks)**

b. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals. **(08 Marks)**

c. Describe with a suitable diagram a digital model for production of speech signal. **(06 Marks)**

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