

# CBCS SCHEME



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15EC663

## Sixth Semester B.E. Degree Examination, June/July 2018 Digital System Design Using Verilog

Time: 3 hrs.

Max. Marks: 80

**Note:** Answer FIVE full questions, choosing one full question from each module.

### Module-1

- 1 a. What are the two sources of power consumption in digital components? Explain. (04 Marks)
- b. Develop a verilog model for a 4 : 1 multiplexer. (04 Marks)
- c. Design an encoder for the buglar alarm that has sensors for each of the 8 zones as a priority encoder with zone 1 having highest priority down to zone 8 having lowest priority. (08 Marks)

OR

- 2 a. Explain the simple design methodology followed in IC industry. (08 Marks)
- b. Develop a datapath to perform complex multiplication of two complex number whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post-binary points. Real and imaginary parts of the product are represented with 8 pre-binary points and 24 post-binary points. Area is the main constraint. Also write the verilog model of the complex multiplier datapath. (08 Marks)

### Module-2

- 3 a. Design a 1m × 8 bit composite memory using 512 K × 8 bit memory component. (04 Marks)
- b. Design a 16K × 48-bit memory using 16K × 16-bit memory component. (04 Marks)
- c. Explain flowthrough and pipelined SSRAM with the help of timing diagram. (08 Marks)

OR

- 4 a. Determine whether there is an error in the ECC word 000111000100 and if so, correct it. (06 Marks)
- b. Develop a verilog model of a dual-port 4K × 16 bit flow through SSRAM. One port allows data to be written and read, while the other port allows data to be read. (06 Marks)
- c. Explain dynamic RAM operation. (04 Marks)

### Module-3

- 5 a. Write and explain the internal organization of a CPLD. (08 Marks)
- b. What are the two main design and manufacturing techniques for ASIC's. Explain. (08 Marks)

OR

- 6 a. Write and explain the internal organization of FPGA. (08 Marks)
- b. Explain differential signaling in detail. (08 Marks)

### Module-4

- 7 a. Explain Flash ADC and successive approximation ADC with the help of necessary diagrams. (08 Marks)
- b. Design an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the I/P value changes. The controller is the only interrupt source in the system. Also develop a verilog model of the I/P controller. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42-8=50, will be treated as malpractice.



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OR

- 8 a. Explain the following serial interface standards for connecting I/O devices:  
(i) I<sup>2</sup>C (ii) USB (08 Marks)  
b. With a neat diagram, explain R-string DAC and R/2R ladder DAC. (08 Marks)

**Module-5**

- 9 a. Explain the design flow of hardware/software co-design. (10 Marks)  
b. Explain floorplan, placement and routing of ASIC physical design. (06 Marks)

OR

- 10 a. Explain Built-In Self Test (BIST) techniques. (08 Marks)  
b. Explain the terms scan design and boundary scan. (08 Marks)

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