CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the following constraints imposed in real world circuits : (i) Noise margin (ii) Static levels (iii) Propagation delay (iv) Static and dynamic power consumption. **(08 Marks)**

b. Explain with illustration a simple methodology followed in IC industries. **(08 Marks)**

OR

2 a. Develop a verilog model for a 7 segment decoder. **(05 Marks)**

b. Develop a verilog model of a debouncer for a push button switch that uses a debouncer interval of 10 mS. Assume the system clock frequency is 50 MHz. **(05 Marks)**

c. Write a brief notes on finite state machine. **(06 Marks)**

Module-2

3 a. Design a 64 K * 8 bit composite memory using four 16 K×8 bit components. **(06 Marks)**

b. Explain the different ROM's used in digital system. **(06 Marks)**

c. Compute the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

OR

4 a. Explain briefly about asynchronous static RAM. **(08 Marks)**

b. Develop a verilog model of a dual port, 4K ×16bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(05 Marks)**

c. Write a note on DRAM. **(03 Marks)**

Module-3

5 a. Explain briefly about the sequence of steps involved in IC manufacture. **(06 Marks)**

b. What are the distinguishes between a plat form FPGA from a simple FPGA? **(06 Marks)**

c. Explain the differential signaling. **(04 Marks)**

OR

6 a. Write a note on complex PLDs. **(08 Marks)**

b. Explain briefly about the internal organization of an FPGA with a neat diagram. **(08 Marks)**

Module-4

7 a. Explain the analog inputs used in input devices. **(04 Marks)**

b. Explain any four serial interface standards. **(08 Marks)**

c. Explain briefly the tristate buses and weak keepers. **(04 Marks)**