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10EC63

Sixth Semester B.E. Degree Examination, June/July 2018
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any THREE full questions from Part-A and any TWO full questions from Part-B.***

PART – A

1 a. Discuss the VI characteristics of the n-MOSFET in different regions by deriving i_D - V_{DS} relationship equation. **(12 Marks)**

b. Consider the circuit given in Fig.Q1(b). Let the voltage V_D be applied to the gate of another transistor for Q_2 as shown in Fig.Q1(b). Assume Q_1 and Q_2 are identical and $\lambda = 0$. Find the drain current and voltage of Q_2 and R at Q_1. Let $V_{DD} = 5V$, $V_t = 0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $L = 0.8\ \mu m$, $\omega = 4\ \mu m$, $V_{OV} = 0.4\ V$. **(08 Marks)**

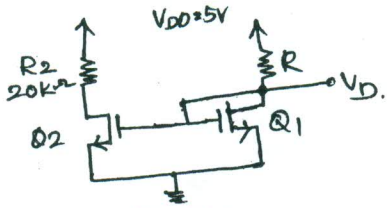

Fig.Q1(b)

2 a. Characterize the common source single stage amplifier with and without source degeneration circuit by deriving the amplifier parameters of R_{in}, V_i, V_o, A_V, A_{VO}, R_{out} and G_{VO}. **(10 Marks)**

b. Consider the circuit given in below Fig.Q2(b) to establish a dc current of $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V, $K'W/L = 1$ mA/V^2. Let $\lambda = 0$, $V_{DD} = 15V$. If instead of given circuit fixed – Vgs bias circuit is used then find the value of required Vgs to establish $I_D = 0.5$ mA. Calculate in both the type of biasing circuits the percentage change in the value of I_D obtained when MOSFET is replaced with another unit having the same K(W/L) but $V_t = 1.5V$. [Hint : Choose R_D and R_S to provide 1/3 of V_{DD} as a drop across them]. **(10 Marks)**

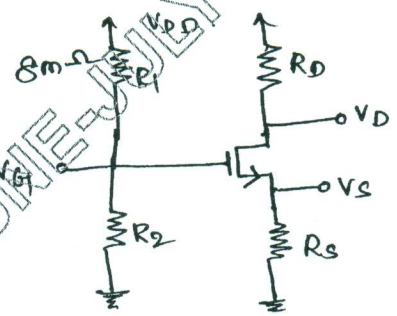

Fig.Q2(b)

3 a. What do you understand about current steering process? Draw and explain a BJT current steering circuit to generate number of constant currents of various magnitudes. **(07 Marks)**

b. What are the different short channel effects? **(05 Marks)**

c. For the given circuit in Fig.Q3(c) find the width of all the transistors. Let $V_{DD} = V_{SS} = 3V$, $V_{tn} = 0.6V$, $V_{tp} = -0.6V$, and all the channel length $L = 1\ \mu m$, $K_n = 200\ \mu A/V^2$, $K_P = 80\ \mu A/V^2$, $I_{ref} = 10\ \mu A$, $I_2 = 80\ \mu A$, $I_3 = 40\mu A$, $I_5 = 70\ \mu A$, and $\lambda = 0$. The required voltage at the drain of Q_2 allowed to go down to within 0.3V of negative supply and that the voltage at the drain of Q_5 be allowed to go upto 0.2 V of the positive supply. **(08 Marks)**

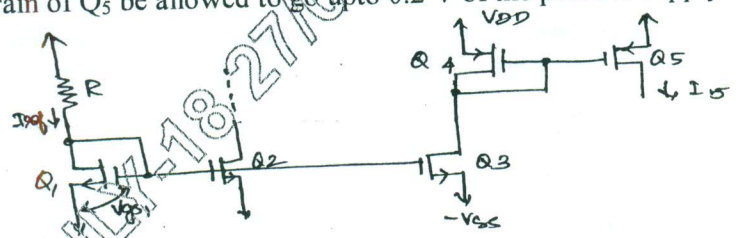

Fig.Q3(c)

4 a. Draw the circuit of common gate amplifier with its active loads. Discuss the small signal analysis and high frequency response. **(10 Marks)**

b. What are two different parameters that decides the performance of the current mirror. Explain the BJT Wilson current mirror circuit and compare it with cascode current mirror. **(06 Marks)**

c. Design Widler current source circuit for generating a constant current $I_o = 10\ \mu A$ which operate from a 10V supply. Determine the values of the required resistors assuming V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β. **(04 Marks)**

5 a. Draw the circuit diagram and different stages of two stage CMOS op-amp and explain its structure with all its parameters. **(10 Marks)**

b. Discuss the large signal and small signal operation of the MOS differential pair. **(10 Marks)**

PART – B

6 a. Explain the different amplifiers to describe the four different feedback topologies. **(10 Marks)**

b. What do you understand about the frequency compensation method of an amplifier to maintain stability for desired value of gain? **(10 Marks)**

7 a. What are the different non-linear functional op-amp circuits? Explain them by deriving the expression for its output voltage. **(10 Marks)**

b. What are the limitations on the performance of op-amp circuits at large o/p signals? **(07 Marks)**

c. Design an inverting amplifier using op-amp having a gain of – 10 and input resistance of 100 kΩ. **(03 Marks)**

8 a. Implement the CMOS logic circuit for the expression $y = A + B(C + DE)$. Provide the W/L ratios of all n-transistor in your circuit, with proper transistor sizing. Assume that for the basic inverter n = 2 and p = 5 and that the channel length is 0.18 μm. **(08 Marks)**

b. Design a level restored n-pass transistor logic circuit for the given expression $Y = A + BC$. Explain the concept of level restoration using your own circuit. **(06 Marks)**

c. Consider a CMOS inverter fabricated in a 0.25 μm process for which $C_{ox} = 6\ fF/\mu m^2$, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $V_{th} = -V_{tp} = 0.4$ V and V_{DD} 2.5 V. The W/L ratio of Q_N is $\frac{0.375\mu m}{0.25\mu m}$, and that for Q_p is $\frac{1.125\mu m}{0.25\mu m}$. The gate-source and gate-drain overlap capacitances are specified to be 0.3 fF/μm of gate width. Further the effective value of drain body capacitances are $C_{dbn} = 1$ fF and $C_{dbp} = 1$ fF. The wiring capacitance $C_W = 0.2$ fF. Find propagation delay t_p. **(06 Marks)**

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