Sixth Semester B.E. Degree Examination, June/July 2016
Microelectronic Circuits

Time: 3 hrs.

Max. Marks:100

Note: *Answer FIVE full questions, selecting*
any Three from Part–A and Two from Part–B.

PART – A

1   a.   Derive the expression of $i_D - V_{DS}$ relationship for triode and saturation region of a NMOS transistor.   **(10 Marks)**

   b.   For the MOSFET with $\dfrac{W}{L} = \dfrac{8\,\mu m}{0.8\,\mu m}$, calculate the values of V_{GS} and V_{DS}(min) needed to operate the transistor in the saturation region with a dc current $I_D = 100$. Assume $K'_n = 194\ \mu A/V^2$ and $V_t = 0.7$ V.   **(05 Marks)**

   c.   Write the expression for the relationship between V_{SB} and V_t. Mention the effect of V_{SB} on the channel.   **(05 Marks)**

2   a.   What are the benefits of short channel MOSFETs?   **(06 Marks)**

   b.   Explain the operation of a MOSFET current mirror.   **(06 Marks)**

   c.   Draw the circuit of a MOS current steering circuit and explain it.   **(08 Marks)**

3   a.   Explain CMOS implementation of the common source amplifier and also draw its i-v characteristic of the active load and transfer characteristic.   **(10 Marks)**

   b.   Consider a common gate amplifier specified as follows :
$\dfrac{W}{L} = \dfrac{7.2\mu m}{0.36\mu m}$. $\mu_n C_{OX} = 387\,\mu A/V^2$, $\gamma_0 = 18$ KΩ, $I_D = 100\ \mu A$, $g_m = 1.25$ mA/V, $\chi = 0.2$, $R_S = 10$ KΩ, $R_L = 100$ KΩ, $C_{gs} = 20$ fF, $C_{gd} = 5$ fF and $C_L = 0$. Find A_{VO}, R_{in}, R_{out}, G_V, G_{is}, G_i and f_H.   **(10 Marks)**

4   a.   What is cascade amplifier? Mention the basic idea behind it.   **(04 Marks)**

   b.   Derive the expression of voltage gain and open circuit voltage gain of a IC-source follower. Draw its small signal equivalent circuit model.   **(08 Marks)**

   c.   Explain the operation of a MOS differential pair with common-mode input voltage.   **(08 Marks)**

5   a.   Explain the operation of a two-stage CMOS op-amp configuration. Mention its features.   **(10 Marks)**

   b.   Illustrate the method of differential to single-ended conversion.   **(07 Marks)**

   c.   What are the factors contribute to the dc offset voltage of the MOS differential pair?   **(03 Marks)**

PART – B

6   a.   Discuss the properties of negative feedback in details.   **(08 Marks)**

   b.   Explain the relationship between stability and pole location of an amplifier with effects.   **(06 Marks)**

   c.   Draw the block diagram, representation of a series-shunt feedback amplifier and derive the expression of input resistance with feedback.   **(06 Marks)**

7 a. Design a non-inverting amplifier with a gain of 2. At the maximum output voltage of 10 V and the current in the voltage divider is to be 10 μA. **(05 Marks)**

    b. With a mathematical analysis and circuits, explain the temperature effects in Logarithmic amplifier are to be minimized. **(09 Marks)**

    c. Draw the sample and hold circuit using op-amp and explain it. **(06 Marks)**

8 a. Define the following parameters of a logic circuit family and write the expressions :
      i) Propagation delay.
      ii) Robustness
      iii) Delay-power product.
      iv) Dynamic power dissipation. **(08 Marks)**

    b. Implement :
      i) $F = \overline{AB + CD}$ using the AND-OR-INVERT gate logic.
      ii) $F = \overline{(A + B)(C + D)}$ using the OR-AND-INVERT gate logic. **(12 Marks)**

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