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10EC63

Sixth Semester B.E. Degree Examination, June/July 2015
Microelectronics Circuits

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE questions, selecting
 THREE from Part-A and TWO from Part-B.**

PART - A

1.
 - a. Derive the $i_D - V_{DS}$ relationship of a MOSFET for triode and saturation region. (12 Marks)
 - b. For a MOSFET process technology with $W/L = 8 \mu\text{m}/0.8 \mu\text{m}$, $t_{ox} = 8\text{nm}$, $\epsilon_r = 3.9$, $\mu_h = 450 \text{cm}^2/\text{v.s}$ and $v_t = 0.7 \text{V}$.
 - i) Find C_{ox} and K'_n .
 - ii) Calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100 \mu\text{A}$.
 - iii) For the device to operate as a 1000Ω resistor find the value of V_{GS} required for very small V_{DS} . (08 Marks)
2.
 - a. Derive the expression for input resistance, output resistance, voltage gain and overall gain of a grounded source amplifier with a neat diagram. (08 Marks)
 - b. Design the biasing circuit shown in Fig.Q.2(b) to establish a drain current $i_D = 0.5\text{mA}$.

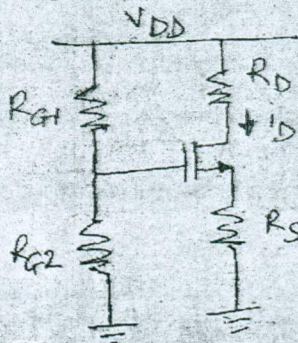


Fig.Q.2(b)

MOSFET has $v_t = 1\text{V}$, $k'_n(W/L) = 1 \text{mA}/\text{V}^2$ and $V_{DD} = 15\text{V}$. Assume one-third V_{DD} across R_D and R_S and neglect channel length modulation $\lambda = 0$. Determine percentage change in value of i_D when MOSFET is replaced with another having $v_t = 1.5\text{V}$. (12 Marks)

3.
 - a. Explain the operation of a MOSFET current steering circuits with necessary expressions. (10 Marks)
 - b. What is MOSFET scaling? Compare MOSFET parameters before and after scaling in constant field scaling and constant voltage scaling. (10 Marks)
4.
 - a. Explain CMOS implementation of CS amplifier and arrive at voltage gain expression $A_v = g_m |r_{o1}|/2$. (10 Marks)
 - b. Derive an expression for the short-circuit transconductance G_m of the MOS cascade amplifier. (10 Marks)

- 5 a. Explain operation of MOS differential pair with common-mode input voltage V_{cm} and determine the highest and lowest value of v_{cm} over which the differential pair operates properly. (08 Marks)
- b. For a MOS differential pair in Fig.Q.5(b).

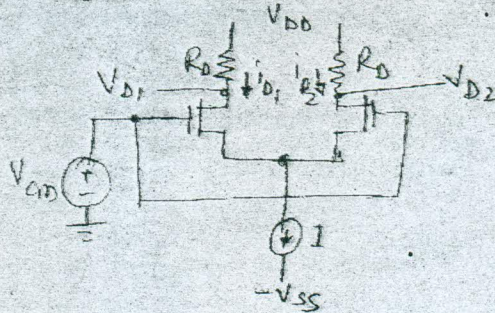


Fig.Q.5(b)

$V_{DD} = V_{SS} = 1.5V$, $k'_n(W/L) = 4mA/V^2$, $v_t = 0.5V$, $I = 0.4mA$, $R_D = 2.5 K\Omega$ neglect channel length modulation.

- Find V_{OV} and V_{GS} for each transistor.
- What is the highest value of V_{an} for Q_1 and Q_2 to remain in saturation?
- If the current source I requires a minimum voltage of $0.4V$ to operate properly what is the lowest value allowed for V_s and V_{an} ? (12 Marks)

PART - B

- Discuss with neat diagram the four basic feedback topologies. (08 Marks)
 - Explain the properties of negative feedback. (08 Marks)
 - What is the general structure of the feedback amplifier? (04 Marks)
- Explain the operation and analysis of single op-amp difference amplifier to determine its common mode gain A_{cm} . (10 Marks)
 - How op-amp circuits can be used as signal integrator and differentiator and determine the time constants? (10 Marks)
- Describe the circuit structure and static operation of CMOS inverter. (08 Marks)
 - With example explain PUN and PDN CMOS logic gate circuits. (08 Marks)
 - Realize two input NOR gate and two input NAND gate using CMOS gate. (04 Marks)
