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10EC63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and TWO from Part-B.***

PART – A

1 a. Draw the physical structure and hence explain the operation of NMOS enhancement type transistor. **(06 Marks)**

b. Derive the expression for drain current i_D in triode and saturation region. **(06 Marks)**

c. Consider a CMOS process for which $L_{min} = 0.8\ \mu m$, $t_{ox} = 15$ nm, $\mu_n = 550\ cm^2/V\text{-}s$ and $V_t = 0.7$ V.

(i) Find C_{ox} and K_n'

(ii) For an NMOS transistor with $\frac{W}{L} = \frac{16\ \mu m}{8\ \mu m}$, calculate the values of V_{OV}, V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a DC current $I_D = 100\ \mu A$.

(iii) For the device in (ii), find the value of V_{OV} and V_{GS} required to cause the device to operate as a 1000 Ω resistor for a very small V_{DS}. **(08 Marks)**

2 a. The NMOS and PMOS transistors in the circuit of Fig.Q2(a) are matched with $K_n'\left(\frac{W_n}{L_n}\right) = K_p'\left(\frac{W_p}{L_p}\right) = 1\ mA/V^2$ and $V_{tn} = -V_{tp} = 1$V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage V_0 for $V_I = 0$ V, +2.5 V, – 2.5V.

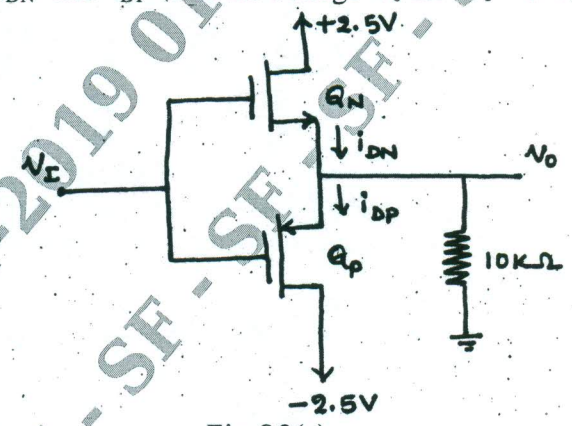

Fig.Q2(a) **(06 Marks)**

b. Draw the circuit diagram of source follower amplifier. Draw its small signal equivalent circuit with r_0. Obtain the expression for V_0, A_V, A_{Vo}, G_V and R_{out}. **(10 Marks)**

c. State and prove Miller's theorem. **(04 Marks)**

3 a. Draw the MOSFET constant current source circuit and explain its operation. **(04 Marks)**

b. Given V_{DD} = 3V and using I_{REF} = 100 μA, it is required to design MOSFET constant current source shown in Fig.Q3(b) to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 μm, channel widths of 10 μm, V_t = 0.7V, and K_n' = 200 μA/V^2. What is the lowest possible value of V_0? Assuming that for this process technology the early voltage V_A' = 20 V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +1V change in V_o

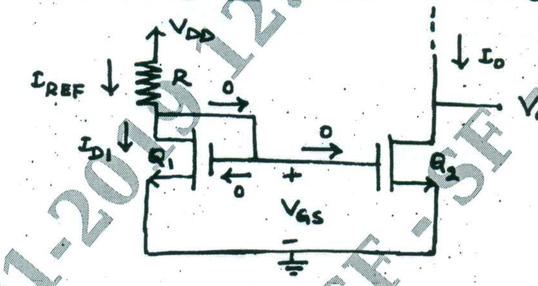

Fig.Q3(b) **(08 Marks)**

c. Explain the operation of a MOS current steering circuit and mention its advantages. **(08 Marks)**

4 a. A CMOS common source amplifier shown in Fig.Q4(a) is fabricated in a 0.18 μm technology has $\frac{W}{L} = \frac{7.2\ \mu m}{0.36\ \mu m}$ for all transistors, K_n' = 387 μA/V^2, K_p' = 86 μA/V^2, I_{REF} = 100 μA, V_{An}' = 5 V/μm and $|V_{Ap}|$ = 6 V/μm. g_{m_1}, r_{01}, r_{02} and the voltage gain.

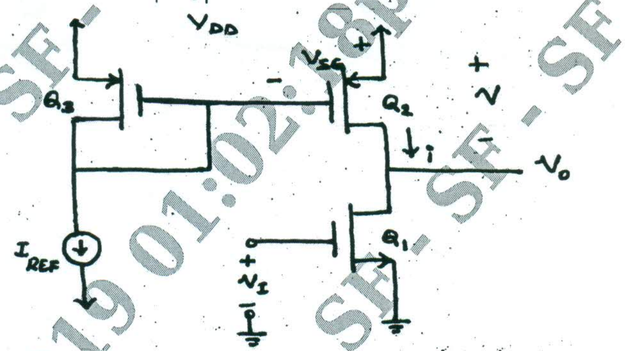

Fig.Q4(a) **(10 Marks)**

b. For the high frequency equivalent circuit for a common source MOSFET amplifier shown in Fig.Q4(b). Derive an expression for 3-dB frequency, f_H using Miller's theorem and open circuit time constant. **(10 Marks)**

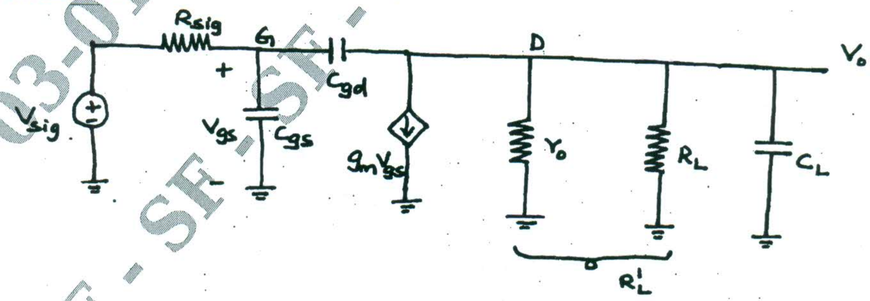

Fig.Q4(b)

5 a. Explain the operation of MOS differential pair with a common mode input voltage. **(04 Marks)**

b. A MOS differential pair is operated at a total bias current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox} = 0.2$ mA/V^2, $V_A = 20$V, and $R_D = 5$ kΩ. Find V_{OV}, g_m, r_o and A_d. **(08 Marks)**

c. With a neat circuit diagram, explain the operation of two stage CMOS operational amplifier configuration. **(08 Marks)**

PART – B

6 a. What are the properties of negative feedback? Explain in more detail. **(06 Marks)**

b. Explain the effect of feedback on the amplifier poles. **(06 Marks)**

c. Discuss the method of frequency compensation for modifying open-loop gain A(s) so that the closed loop amplifier is stable, by introducing a new pole in transfer function at sufficiently low frequency. **(08 Marks)**

7 a. Design an inverting op-amp circuit to form the weighted sum V_0 of two inputs V_1 and V_2. It is required that $V_0 = -(V_1 + 5V_2)$. Choose values for R_1, R_2 and R_f so that for a maximum output of 10 V the current in the feedback resistor will not exceed 1 mA. **(04 Marks)**

b. Explain in detail dc imperfections of an operational amplifier. **(06 Marks)**

c. An op-amp wired in the inverting configuration with the input grounded, having $R_2 = 100$kΩ and $R_1 = 1$ kΩ has an output DC voltage of – 0.3V. If the input bias current is known to be very small, find the input offset voltage. **(04 Marks)**

d. Explain how to minimize the temperature effect in a logarithmic amplifier. **(06 Marks)**

8 a. Explain in detail the static and dynamic operation of a CMOS inverter. **(08 Marks)**

b. Sketch a CMOS realization for the function

$$Y = \overline{A + B(C + D)}$$ **(04 Marks)**

c. Provide transistor $\frac{W}{L}$ ratios for the logic circuit shown in Fig.Q8(c). Assume that for the basic inverter n = 1.5 and p = 5 and that the channel length is 0.25 μm. **(08 Marks)**

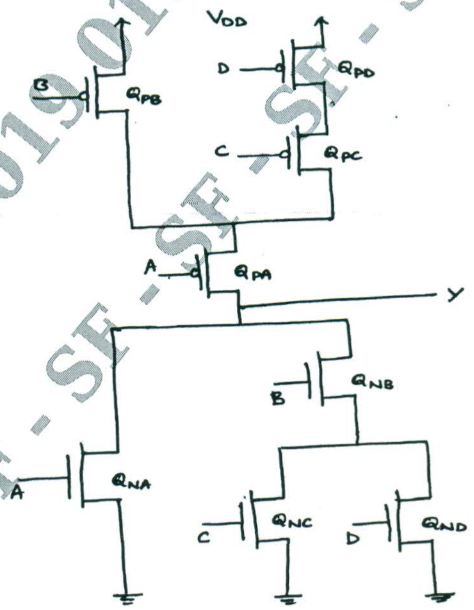

Fig.Q8(c)

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