CBCS SCHEME

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15EC552

Fifth Semester B.E. Degree Examination, June/July 2018
Switching and Finite Automata Theory

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. What is threshold element? Write the symbol for a threshold element. **(04 Marks)**

b. Explain the following :
(i) Magnetic-core threshold element
(ii) Resistor-transistor threshold element. **(06 Marks)**

c. Explain the capabilities and limitations of threshold logic. **(06 Marks)**

OR

2 a. Find the function $f(x_1, x_2, x_3, x_4)$ realized by each of the threshold networks shown in Fig.Q2(a). Show the map of each function. **(10 Marks)**

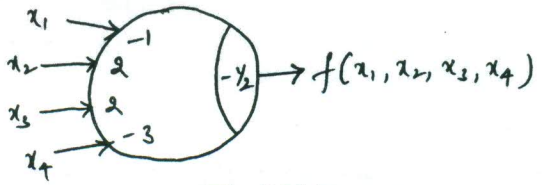

Fig.Q2(a)

b. Explain the following :
(i) Unate functions (ii) Linear Separability. **(06 Marks)**

Module-2

3 a. What is a Static Hazard? Design a hazard-free switching circuit for a function $T(x, y, z) = \Sigma(1, 3, 4, 5)$ **(06 Marks)**

b. Explain the following :
(i) Preset Experiment
(ii) Adaptive Experiment **(10 Marks)**

OR

4 a. What is a Boolean difference? Explain the properties of Boolean differences. **(10 Marks)**

b. Write the fault table for derivation of minimal set of fault-detection test for the following circuit shown in Fig.Q4(b) **(06 Marks)**

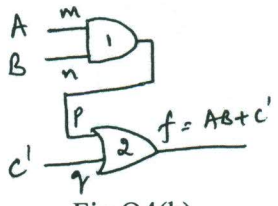

Fig.Q4(b)

Module-3

5 a. What are sequential machines? Explain finite state model and its mathematical representations. **(06 Marks)**

b. What is merger graph? Draw the merger graph for the incompletely specified machine M_1 shown in table Q5(b). **(10 Marks)**

Machine M_1

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	-	C, 1	E, 1	B, 1
B	E, 0	-	-	-
C	F, 0	F, 1	-	-
D	-	-	B, 1	-
E	-	F, 0	A, 0	D, 1
F	C, 0	-	B, 0	C, 1

Table Q5(b)

OR

6 a. Explain the following :
(i) Mealy machine (ii) Moore machine. **(06 Marks)**

b. Draw the merger table for the incompletely specified machine M_2 shown in table Q6(b) and draw the compatibility graph for machine M_2. **(10 Marks)**

Machine M_2

PS	NS, Z	
	I_1	I_2
A	E, 0	B, 0
B	F, 0	A, 0
C	E, -	C, 0
D	F, 1	D, 0
E	C, 1	C, 0
F	D, -	B, 0

Table Q6(b)

Module-4

7 a. Given the machine table in Table Q7(a) M_3 and two assignments α and β, derive in each case the logical equations for the state variables and draw the circuit diagrams of assignments α and β. **(10 Marks)**

Machine M_3

PS	NS		Z	
	x = 0	x = 1	x = 0	x = 1
A	A	D	0	1
B	A	C	0	0
C	C	B	0	0
D	C	A	0	1

Table Q7(a)

	y_1	y_2
A →	0	0
B →	0	1
C →	1	1
D →	1	0

Assignment α

	y_1	y_2
A →	0	0
B →	0	1
C →	1	0
D →	1	1

Assignment β

b. Explain the following :
(i) Output – consistent partition
(ii) Input - consistent partition
(iii) Autonomous clock. **(06 Marks)**