USN | | | | | | | | | | | **15EC53**

Fifth Semester B.E. Degree Examination, June/July 2018
Verilog HDL

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1   a. Explain briefly the typical design flow for design of VLSI circuits.   **(08 Marks)**
    b. Explain the 4 bit ripple carry counter with block diagram and design hierarchy.   **(08 Marks)**

OR

2   a. Explain briefly the two different design methodologies.   **(08 Marks)**
    b. What is an instance? Explain module instantiation with an example.   **(08 Marks)**

Module-2

3   a. Explain the following data types in verilog with an example for each:
        i) Nets   ii) Registers   iii) Memories   iv) Parameters   **(08 Marks)**
    b. Explain monitoring, stopping and finishing in a simulation and also compiler directives.
                                                                                       (08 Marks)

OR

4   a. Write a note on following lexical conventions used in verilog:
        i) Operators   ii) Identifiers and keywords
        iii) Escaped identifiers   iv) Strings   **(08 Marks)**
    b. Explain different methods of connecting ports to external signals.   **(08 Marks)**

Module-3

5   a. Explain the following operators used in verilog with an example.
        i) Logical   ii) Replication   iii) Shift   iv) Conditional   **(08 Marks)**
    b. Write the verilog code and stimulus for gate level 4:1 multiplexer with their logical diagram.
                                                                                       (08 Marks)

OR

6   a. Write the gate level description for 4 bit ripple carry full adder.   **(06 Marks)**
    b. Define bufif/notif and write gate instantiation of bufif, notif gates.   **(04 Marks)**
    c. Define implicit continous assignment delay and net declaration delay with an example.
                                                                                       (06 Marks)

Module-4

7   a. Explain blocking and non-blocking assignments in behavioural description with an example.
                                                                                       (08 Marks)
    b. Explain structured procedures in behavioural description with example.   **(08 Marks)**

OR

8   a. Explain different types of event based timing control in verilog.   **(08 Marks)**
    b. Explain with an example the two types of blocks in verilog behavioural description.
                                                                                       (08 Marks)

Module-5

9   a. Explain the synthesis process with a block diagram.   **(08 Marks)**
    b. Explain the attributes in VHDL with examples.   **(08 Marks)**

OR

10 a. Explain simulate the post fit design implementation in VHDL.   **(08 Marks)**
    b. Explain different scalar types in VHDL.   **(08 Marks)**

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