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10EC56

Fifth Semester B.E. Degree Examination, June/July 2016
Fundamentals of CMOS VLSI

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART - A

- Discuss latch-up in a p-well CMOS structure and its remedies. With neat figure explain twin tub CMOS process steps. (10 Marks)
 - For an NMOSFET, the following details are available $\mu_n = 500\text{cm}^2/\text{V-se}$, $(V_a - V_{tn}) = 2.6\text{V}$, $t_{ox} = 100 \text{ \AA}$. Calculate R_n of the device if $w = 100\mu\text{m}$, $L = 0.5\mu\text{m}$. (05 Marks)
 - Deduce an equation for figure of merit of MOS transistor. Find the operating frequency f_o in the following condition $\mu_n = 125\text{cm}^2/\text{v-sec}$, $L = 2 \mu\text{m}$, $V_{gs} = 2\text{V}$ and $\mu_{tn} = 1\text{V}$. (05 Marks)
- What are the uses of stick diagram? Give the table of color and monochrome stick encoding for simple single metal NMOS process. (07 Marks)
 - Draw the CMOS circuit diagram, stick diagram and symbolic diagram of Boolean function $F = \overline{wx} + yz$. (06 Marks)
 - What do you mean by λ based design rule? Explain λ based design rules applicable to MOS layers and transistors. (07 Marks)
- With neat circuit diagram explain the following : (i) A simple BiCMOS inverter and (ii) An improved BiCMOS inverter with no static current flow and better output logic levels. (10 Marks)
 - Draw and explain the basic structure of dynamic CMOS logic and discuss the charging sharing problem in this structure. (10 Marks)
- What are the most commonly used scaling models? Provide scaling factors for (i) power dissipation per gate (ii) Gate delay (iii) current density and (iv) speed power product. (10 Marks)
 - For the given multilayer structure shown in Fig. Q4(b) calculate the total capacitance. (10 Marks)

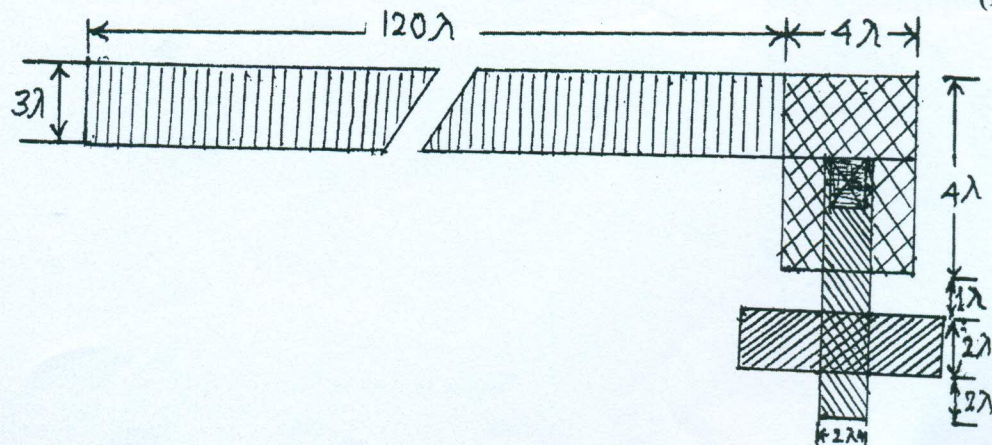


Fig. Q4(b)



PART – B

- 5 a. Obtain switch logic arrangements for (i) $V_{out} = V_1A + V_2B + V_3C$ using 3 way selector switch and (ii) 3 input nMOS OR gate. (10 Marks)
- b. Draw and explain 4 : 1 MUX using transmission gate. (05 Marks)
- c. Explain with neat figure, non – inverting dynamic storage cells using CMOS transmission gate switch. (05 Marks)

- 6 a. With the help of logic expressions explain how to implement arithmetic logic operations with a standard adder. (10 Marks)
- b. Explain with neat diagram the 4×4 cross bar switch. (10 Marks)

- 7 a. With neat figure explain transistor dynamic RAM cell. (06 Marks)
- b. Describe the CMOS pseudo static memory cell with neat figure. (06 Marks)
- c. Explain read and write operations in dynamic memory cell. (08 Marks)

- 8 Write short notes on :
 - a. Input/output pads (05 Marks)
 - b. Test and Testability. (05 Marks)
 - c. Level sensitive scan design and (05 Marks)
 - d. Built in self test (BIST). (05 Marks)

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