USN | | | | | | | | | | **10EC56**

Fifth Semester B.E. Degree Examination, Dec.2015/Jan.2016
Fundamentals of CMOS VLSI

Time: 3 hrs.   Max. Marks:100

Note: 1. *Answer FIVE full questions, selecting at least TWO questions from each part.*
2. Assume missing data, if any.

PART – A

1 a. Explain with a neat diagram, enhancement mode transistor action of MOS transistor.
                                                                      (08 Marks)
   b. Using neat diagram, describe fabrication steps for n-MOS transistor.   **(08 Marks)**
   c. Compare CMOS and Bipolar technologies.   **(04 Marks)**

2 a. What do you mean by Lambda (λ) based design rule? Explain, indicate and draw design rule for PMOS, CMOS and n-mos.   **(12 Marks)**
   b. Using CMOS logic draw schematic and Layout diagram for $Y = \overline{AB + CD}$.   **(08 Marks)**

3 a. Explain why p-MOS and n–MOS has been used in CMOS complementary logic. Discuss CMOS complementary logic with an example.   **(06 Marks)**
   b. Describe the following logic structures with an example.
        i) Pseudo – n-MOS logic
        ii) Dynamic CMOS logic   **(10 Marks)**
   c. Using Bi-CMOS logic structure design a schematic circuit for $h = \overline{ab + c}$.   **(04 Marks)**

4 a. What is sheet resistance? Derive the expression for sheet resistance.   **(08 Marks)**
   b. Explain delay unit.   **(06 Marks)**
   c. Discuss the scaling factors for n-MOS transistor.   **(06 Marks)**

PART – B

5 a. Discuss the architectural issues of CMOS subsystem design.   **(04 Marks)**
   b. Explain combinational logic using a parity generator.   **(08 Marks)**
   c. Explain: i) Dynamic register element   ii) Dynamic shift register.   **(08 Marks)**

6 a. Design and explain 4bit shifter using 4×4 cross bar and barrel shifter.   **(12 Marks)**
   b. Explain with a neat diagram 4 – bit serial – parallel multiplier.   **(08 Marks)**

7 a. Explain with a neat diagram, a three transistor dynamic RAM cell.   **(08 Marks)**
   b. Explain CMOS Pseudo – static memory cell using circuit and stick diagram.   **(12 Marks)**

8 a. Discuss the floor plan and layout using 4 – bit processor.   **(08 Marks)**
   b. Write a short note on
        i) Built – in – self – test (BIST)
        ii) Scan design technology.
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