CBCS SCHEME

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15EC46

Fourth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define the following terms as applied to Op-Amp and mention their typical values for IC 741. i) CMRR ii) Slew rate iii) PSRR. **(06 Marks)**

b. With a neat circuit diagram explain the basic Op-Amp circuit. **(06 Marks)**

c. An operational amplifier has a specified input voltage range of ± 8V and an output voltage range of ±14V when the supply voltage is ±15V. Calculate the maximum output voltage that can be produced i) When the Op-Amp is used as a voltage follower ii) When it is used as an amplifier with a voltage gain of 2. **(04 Marks)**

OR

2 a. With a neat circuit diagram, explain direct coupled inverting amplifier with design steps, input impedance and output impedance. **(08 Marks)**

b. Derive an output voltage equation of 3 input inverting summing circuit and show how it can be converted into averaging circuit. **(08 Marks)**

Module-2

3 a. Explain capacitor coupled voltage follower with neat circuit diagram. **(08 Marks)**

b. Design a capacitor coupled non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15mV. The load resistor is 2.2 kΩ and the lower cutoff frequency is to be 120Hz. **(08 Marks)**

OR

4 a. Explain the circuit operation of a differential input/output amplifier and derive the equation for differential voltage gain. Also show that the common mode gain is unity. **(10 Marks)**

b. Design a non-saturating precision half wave rectifier to produce a 2V peak output from a sine wave input with a peak value of 0.5V and frequency of 1MHz. Use a bipolar Op-Amp with supply voltage of ±15V. **(06 Marks)**

Module-3

5 a. With neat circuit diagram and waveforms, explain sample and hold circuit. **(08 Marks)**

b. Explain differentiating circuit operation with neat circuit diagram and design steps. **(08 Marks)**

OR

6 a. Using 741 Op-Amp with a supply of ±12V, design a phase shift oscillator to have an output frequency of 3.5KHz. **(06 Marks)**

b. Explain log amplifier and derive its output voltage equation. **(06 Marks)**

c. Using a 741 Op-Amp with supply voltage of ± 12V, design an inverting Schmitt trigger circuit to have trigger points of ± 2V. **(04 Marks)**

Module-4

7 a. Explain the operation of second order high pass filter with a neat circuit diagram, frequency response and design steps. **(08 Marks)**

b. With a neat diagram and design steps explain the operation of single stage first order bandpass filter. **(08 Marks)**

OR

8 a. With a neat sketch, explain the working of series Op-Amp regulator. **(06 Marks)**

b. List and explain the characteristics of 3 terminal IC regulators. **(04 Marks)**

c. Draw and explain functional diagram of 723 regulators. **(06 Marks)**

Module-5

9 a. Define the following in relation to PLL :
i) Lock in range ii) Capture range iii) Pull in time. **(06 Marks)**

b. With necessary circuit diagram, derive the equations and explain R – 2R DAC. What output voltage could be produced by a DAC whose output range is 0 to 10V and whose input binary number is i) 11(for 2 bit DAC) ii) 1011 (for 4 bit DAC). **(10 Marks)**

OR

10 a. Explain the operation of monostable multivibrator using 555 timer. **(08 Marks)**

b. In the satable multivibrator $R_A = 3.3k\Omega$ $R_B = 6.8k\Omega$ and $C = 0.01\ \mu F$. Calculate :
i) t_{High} ii) t_{low} iii) free running frequency iv) duty cycle D. **(08 Marks)**

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