CBCS SCHEME

USN | | | | | | | | | | | **15EC46**

Fourth Semester B.E. Degree Examination, Dec.2018/Jan.2019

Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. Missing data may be assumed with necessary justification.

Module-1

1 a. List the ideal electrical characteristics of operational amplifier and mention the practical values for each. **(05 Marks)**

b. Explain the operation of direct coupled non-investing summing amplifier and show that output voltage $V_0 = V_1 + V_2$ with necessary proof. **(05 Marks)**

c. Design an direct coupled inverting amplifier using op-amp 741 with voltage gain 100 and output voltage required is 5V. **(06 Marks)**

OR

2 a. Explain the following terms : i) input offset voltage ii) slew rate iii) output voltage swing iv) CMRR v) PSRR.
Mention the typical values of each terms for 741 op-amp. **(05 Marks)**

b. Discuss the ideal voltage transfer curve of op-amp and also draw the equivalent circuit of op-amp and discuss it significance. **(05 Marks)**

c. Sketch the direct coupled difference amplifier circuit. Derive an equation for output voltage (ie $V_0 = \frac{R_2}{R_1}(V_2 - V_1)$) and explain the operation. **(06 Marks)**

Module-2

3 a. Sketch the circuit of a high Z_{in} capacitor coupled voltage follower. Briefly explain its operation and show that the input impedance is very high compared to the capacitor coupled voltage follower. **(05 Marks)**

b. Design capacitor coupled non-inverting amplifier to have voltage gain of 66. The signal amplitude is of 25mV. The load resistor is 2.2kΩ and lower cut-off frequency is to be 120Hz. Sketch the circuit. **(05 Marks)**

c. Design a capacitor coupled inverting amplifier to operate with a +20V supply. The minimum input signal level is 50mV, the voltage is to be 68, the load resistance is 500 ohms, the lowest cutoff frequency is to be 200Hz. Use 741 op-amp with maximum input bias current $I_{B(max)} = 500nA$. **(06 Marks)**

OR

4 a. Sketch the circuit of 3-op-amp instrumentation amplifier and explain its operation and with necessary proof show that $V_0 = \frac{R_2}{R_1}\left[1 + \frac{2R_f}{R_G}\right](V_2 - V_1)$. And also list the requirements of instrumentation amplifier. **(10 Marks)**

b. Sketch the precision full wave rectifier and explain the operation with necessary mathematical equations and waveforms. **(06 Marks)**

Module-3

5 a. Draw the circuit diagram of inverting Schmitt trigger with different UTP and LTP adjustments. Sketch I/O transfer curve and waveform and the operation. **(10 Marks)**

b. Using 741 op-amp with supply of ±12V, design a RC phase shift oscillator to have an output frequency of oscillation 5KHz. Choose $I_1 = 50\ \mu A$. **(06 Marks)**

OR

6 a. Draw the detailed circuit diagram of sample and hold circuit and explain the operation with necessary waveforms. **(05 Marks)**

b. Sketch the circuit and explain the operation of voltage to current converter with grounded load and show that load current is independent of R_L. **(05 Marks)**

c. Design the capacitor coupled zero- crossing detector using op-amp 741 having $I_{B(max)}$ = 500nA and minimum signal frequency is 500Hz. The supply voltages are ±12V. **(06 Marks)**

Module-4

7 a. Design a first order high pass filter with f_L = 10KHz with passband gain of 1.5 and also plot the frequency response of designed filter. **(06 Marks)**

b. Show how ban stop filter circuit can be constructed by using LPF and HPF. Sketch the block diagram and explain with necessary waveform. **(06 Marks)**

c. Draw the ideal response curves for all types of filters and briefly explain. **(04 Marks)**

OR

8 a. List the performance parameters of power supply and explain. **(05 Marks)**

b. With necessary functional block diagram of 3-terminal IC voltage regulator explain its operation. **(05 Marks)**

c. Draw the circuit of wide band pass filter and explain its operation. Sketch the necessary wave forms also. **(06 Marks)**

Module-5

9 a. Draw the block diagram of PLL and explain its operation, list the application of PLL. **(05 Marks)**

b. Explain the operation of analog to digital conversion using successive approximation technique. **(05 Marks)**

c. Design astable multivibration using 555 timer for the frequency of oscillation 2KHz with 25% duty cycle. Sketch the circuit after design. **(06 Marks)**

OR

10 a. With necessary circuit, explain how PLL can be used as frequency multiplier and divider. **(05 Marks)**

b. Explain how 4-bit digital information converted to analoge using R-2R ladder N/w DAC. **(05 Marks)**

c. List the specification parameters of ADC and briefly discuss on same (min 4 parameters). **(06 Marks)**

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