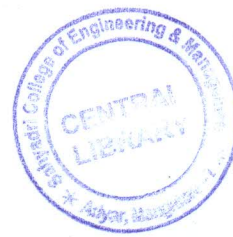


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**Fourth Semester B.E. Degree Examination, June/July 2015**  
**Linear Integrated Circuits and Applications**

Time: 3 hrs.

Max. Marks: 100

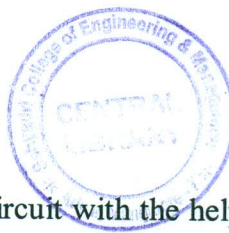
**Note: Answer any FIVE full questions, selecting  
atleast TWO questions from each part.**

**PART – A**

- 1
  - a. Explain the working of a basic operational amplifier circuit with  $R_c = 7.5 \text{ K}\Omega$ ,  $R_E = 3.8 \text{ K}\Omega$  and powered by  $\pm 12\text{V}$  supply. (08 Marks)
  - b. Design a bias-current compensated inverting amplifier to amplify a dc input of 150 mV by a factor of 40. Use a bipolar op-amp with  $I_{B_{\max}} = 500 \text{ nA}$ . (06 Marks)
  - c. Derive an expression to relate the input and output common mode voltage ( $V_{icm}$  and  $V_{ocm}$ ) of a non-inverting amplifier. (06 Marks)
  
- 2
  - a. Explain the realization of a C-coupled voltage follower for AC amplifier applications, discussing cut-off frequency design concept. (06 Marks)
  - b. Design a BIFET op-amp based high input impedance C-coupled non-inverting amplifier for a lower cut-off frequency of 120 Hz. Given:  $V_{in} = 20 \text{ mV}$ ,  $V_0 = 5\text{V}$  and  $R_{L_{\min}} = 10\text{K}\Omega$ . (08 Marks)
  - c. Explain the concept and construction of a C-coupled inverting amplifier using a single-polarity supply ( $+V_{cc}$ ). (06 Marks)
  
- 3
  - a. Considering the frequency and phase responses of an uncompensated op-amp with a three-stage model, discuss the concept of circuit stability. (10 Marks)
  - b. Explain frequency compensation based on Miller effect, also explaining the capacitance-amplification principle. (06 Marks)
  - c. A voltage follower is to operate at a unity gain bandwidth of 1 MHz, and the op-amp has a slew rate of  $0.75 \text{ V}/\mu\text{s}$ . Determine the permissible peak output voltage, and the cut-off frequency related rise time. (04 Marks)
  
- 4
  - a. Design a current source to produce an output of 150 mA to a grounded load of maximum value  $30 \Omega$ . Use an op-amp with  $\pm 12\text{V}$  supply and a power MOSFET with  $R_{D_{\text{on}}} = 6\Omega$  as the current booster. (08 Marks)
  - b. Derive an expression for the differential gain of an instrumentation amplifier. (06 Marks)
  - c. Explaining the operation briefly, design a non-saturating half wave precision rectifier to produce a 3 Volt peak output from an input of peak value 0.25 V, and frequency of 5 kHz. Use a bipolar op-amp with  $\pm 15\text{V}$  power supply. (06 Marks)

**PART – B**

- 5
  - a. Explain the operation of a voltage follower peak detector circuit, discussing capacitor selection procedure. (08 Marks)
  - b. Design an RC-phase shift oscillator to generate sustained oscillations at a frequency of 1.5 kHz. Use a 741 op-amp and  $\pm 12\text{V}$  power supply. (06 Marks)
  - c. Deriving an expression, discuss the fundamental log-amplifier circuit. (06 Marks)



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- 6 a. Explain the operation of an inverting Schmitt trigger circuit with the help of waveforms and transfer characteristics. (08 Marks)
- b. Design an op-amp based monostable multivibrator to generate a pulse of width  $PW = 2ms$ . The trigger is a pulse of amplitude 3V and duration 150  $\mu s$ . Use a bipolar op-amp and a supply of  $\pm 12V$ . (08 Marks)
- c. Design a first order high pass active filter for a cut-off frequency of 2 kHz. (04 Marks)
- 7 a. Briefly explain the operation of a series voltage regulator. (06 Marks)
- b. Design a voltage regulator circuit using LM723 to obtain  $V_0 = 5V$ , and  $I_0 = 2A$ . (06 Marks)
- c. Explain the basic principle of operation of switching regulators. Also list any four merits. (08 Marks)
- 8 a. Design an astable multivibrator using 555 timer to obtain a square wave of frequency 5 kHz at 50% duty cycle. (06 Marks)
- b. Discuss the operating principle of PLLS and define the lock-in and capture ranges. (08 Marks)
- c. Explain the binary weighted technique of digital to analog conversion. What is its major disadvantage? (06 Marks)

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