Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Linear ICs and Applications

Time: 3 hrs.

Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting
atleast TWO questions from each part.
2. Use of standard resistor value and standard
capacitor value table is allowed.*

PART – A

1 a. Define the following terms with respect to opamp and specify their typical values for a 741 opamp:
   i) CMRR   ii) PSRR   iii) Slew Rate.   **(06 Marks)**
   b. Derive an expression for the output voltage of non-inverting summing circuit.   **(07 Marks)**
   c. The difference of two input signals is to be amplified by a factor of 37. Each input has an amplitude of approximately 50 mV. Using LF353 opamp, design a difference amplifier to obtain approximately equal input resistance at the two input terminals and also provide common mode nulling.   **(07 Marks)**

2 a. Using a BIFET opamp, design a capacitor coupled inverting amplifier with an input signal of 30 mV, a load resistance of 2.2 kΩ, $A_V = 150$ and $f_l = 80$ Hz.   **(05 Marks)**
   b. A high input impedance capacitor coupled non-inverting amplifier is to be designed using 741 opamp with $A_V = 120$, $f_l = 100$ Hz, input signal of 50 mV, and the load resistance ranging from 2.7 kΩ to 27 kΩ.   **(09 Marks)**
   c. Using 741 opamp with maximum input bias current of 500 nA, design a capacitor coupled voltage follower with a lower cutoff frequency of 120 Hz, and load resistance of 8.2 kΩ using +30V power supply.   **(06 Marks)**

3 a. Discuss about the conditions that have to be fulfilled for an opamp circuit to oscillate.   **(05 Marks)**
   b. With the help of circuit schematic and frequency response, explain how phase lag compensation can be used to stabilize opamp circuit.   **(05 Marks)**
   c. Mention the need for Z_{in} MOD compensation. Discuss the role of compensating components in Z_{in} MOD compensation for an inverting amplifier.   **(05 Marks)**
   d. List the precautions to be observed for opamp circuit stability.   **(05 Marks)**

4 a. Design a low resistance voltage source (with reference voltage derived from potential divider) to provide an output voltage of 8V. A 741 opamp with a ±15V supply is to be used, and the maximum output current is to be 60 mA.   **(08 Marks)**
   b. Determine the range of resistance of externally connected resistor R_G for a LH0036 IC instrumentation amplifier to give a voltage gain adjustable from 30 to 300.   **(03 Marks)**
   c. Design a precision full wave rectifier consisting of a summing circuit and a precision half wave rectifier to produce a 2V peak output from a sine wave input with peak value of 0.5 V and frequency of 1 MHz. Use bipolar opamps with a supply voltage of ±15V.   **(09 Marks)**

PART – B

5   a.   A ±5V, 10 kHz square wave from a signal source with a resistance of 100 Ω is to have its positive peak clamped precisely at ground level. Tilt on the output is not to exceed 1% of the peak amplitude of the wave. Design the precision clamping circuit using a supply of ±12V.   **(08 Marks)**

   b.   Draw the fundamental circuit of logarithmic amplifier and derive an expression for output voltage.   **(06 Marks)**

   c.   Design a wein bridge oscillator to have an output frequency of 15 kHz using a BIFET opamp with a supply voltage of ±12V.   **(06 Marks)**

6   a.   With a neat circuit diagram and associated waveforms explain the working principle of inverting Schmitt trigger circuit.   **(05 Marks)**

   b.   Explain the working principle of astable multivibrator with a neat circuit schematic and waveforms. Specify the design procedure for this circuit.   **(09 Marks)**

   c.   Using a 741 opamp, design a second order low pass filter with a cutoff frequency of 1 kHz.   **(06 Marks)**

7   a.   Discuss about the important characteristics of three terminal IC regulator.   **(04 Marks)**

   b.   Draw the functional block diagram of IC723 voltage regulator and explain.   **(06 Marks)**

   c.   With the help of circuit schematic explain the principle of operation of switched mode power supply. Mention its advantages.   **(10 Marks)**

8   a.   Draw the circuit diagram of monostable multivibrator using IC 555 and derive the expression for output pulse width.   **(05 Marks)**

   b.   Give the basic block schematic of PLL and explain the function of each block.   **(06 Marks)**

   c.   Draw the functional diagram of dual slope ADC and explain its working principle. Mention its advantages and limitations.   **(09 Marks)**

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