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Fourth Semester B.E. Degree Examination, June/July 2017
Fundamentals of HDL

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART - A

- 1
 - a. Explain in brief verilog data types and operators with example. (11 Marks)
 - b. List different modeling styles. Define significances of each modeling style. (06 Marks)
 - c. Find the value of expression X_1 , X_2 , X_3 for the following VHDL signal declaration,
 Signal a : bit := '1' ;
 Signal b : bit - vector (3 down to 0) := "1010";
 Signal c : bit - vector (0 to 3) := "0010" ;
 $X_1 = C \text{ sll } 2$
 $X_2 = b \text{ sra } 3$
 $X_3 = a \overline{b(2)} \overline{c(1)}$ (03 Marks)
- 2
 - a. Design a 4 : 1 Mux and implement the same using Boolean equation in verilog. (05 Marks)
 - b. Design 3×3 unsigned combinational array multiplier in VHDL assigning a delay 5 ns. (10 Marks)
 - c. Write a verilog description for a SR latch: (i) Use a characteristic equation. (05 Marks)
 (ii) Use two logic gates.
- 3
 - a. architecture sig of dummy is
 Signal trigger, sum : integer := 0 ;
 Signal Sig 1 : integer := 1 ;
 Signal Sig 2 : integer := 2 ;
 Signal Sig 3 : integer := 3 ;
 begin
 process (trigger)
 begin
 Sig 1 \leftarrow Sig2 + Sig3 ; Sig2 \leftarrow Sig1 ;
 Sig 3 \leftarrow Sig2 ; Sum \leftarrow Sig1 + Sig2 + Sig3 ;
 end process; eng Sig ;
 architecture Var of dummy is
 Signal trigger, Sum : integer := 0;
 Begin
 Process (trigger)
 Variable Var 1 : integer := 1 ;
 Variable Var 2 : integer := 2 ;
 Variable Var 3 : integer := 3 ;
 Begin
 Var1 := Var2 + Var3 ; Var 2 := Var 1 ;
 Var3 := Var2 ; Sum \leftarrow Var1 + Var2 + Var3 ;
 end process ; end Var ;
 The trigger value changes at $t = 10 \text{ ns}$, the statements are executed only once.
 Evaluate the value of sum at $t = 10 \text{ ns} + \Delta$ for above 2 cases. (06 Marks)
 - b. Design 4-bit ripple adder using for loop only and implement the same using VHDL. (07 Marks)
 - c. Write a behavioral description in verilog for JK flip flop using if and else if statement only. With active low clock and asynchronous reset. (07 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

- 4 a. Design a 3-bit synchronous even counter using D flip flop with active high hold and implement the same in structural description in verilog. (10 Marks)
- b. Write the HDL programs for N+1 bit magnitude comparator using,
- Generate and generic in VHDL.
 - Generate and Parameter in verilog. (10 Marks)

PART – B

- 5 a. Write a code to convert integer to signed Binary (4 – bit) using procedure. (08 Marks)
- b. Bring out the difference between procedure and function with an example. (07 Marks)
- c. Write a note on verilog file processing. (05 Marks)

- 6 a. Write the block diagram and function table of a SRAM, using this write VHDL description of 16×8 SRAM. (08 Marks)

- b. Package array is

```
Constant P : integer := 2 ;
Constant N : integer := 2 ;
Constant M : integer := 1 ;
```

Subtype wordg is integer ;

```
type Single 1 is array (P downto 0) of wordg ;
type Single 2 is array (N downto 0) of Single 1 ;
type arry 3 is array (M downto 0) of single 2 ;
end array;
```

library IEEE;

Use IEEE.STD-LOGIC-1164.ALL;

Use work.arry.all;

Entity Ex is

```
Part (N, M, P: integer ; z : out integer);
```

End Ex;

Architecture Ex₁ of Ex is

Begin

```
Process (N, M, P)
```

```
Variable t ; integer ;
```

```
Constant y; arry 3:=(((5, 4,3),(8, 9, 10),(32, 33, 34)),((42, 43,44),(52, 53,54),(-10, -7, -5)));
```

begin

```
t := y(M)(N)(P);
```

```
z <= t; end process ; end Ex1;
```

- (i) What is the value of the following element of y?

Y(0, 0, 0), Y(0, 0, 1), Y(0, 0, 2), Y(0, 1, 2), Y(1, 1, 2), Y(1, 2, 2)

- (ii) If we change all (N downto 0) and (M downto 0) in package arry to (0 to N) and (0 to M). What will be the values of the elements in part (i). (08 Marks)

- c. Which line in the above program 6(b) attaches a package to the VHDL program? Explain each word in that line and significance of each word. (04 Marks)

- 7 a. Write mixed-language description of a master slave JK-ff with a clear input invoking a VHDL entity from a verilog module. (12 Marks)
- b. Discuss the facts of the mixed language description. (08 Marks)