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10EC45

Fourth Semester B.E. Degree Examination, June/July 2016
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe VHDL scalar data types with an example. **(08 Marks)**

b. Explain composite and access data types with an example for each. **(08 Marks)**

c. If A, B and C are three unsigned variables with A = 11110000, B = 01011101 and C = 0000 0000 find the value of i) A NAND B ii) A&&C iii) A ror2 iv) B<<1. **(04 Marks)**

2 a. Write a VHDL code in data flow description for a 2 bit magnitude comparator with help of truth table and simplified Boolean expressions. **(12 Marks)**

b. Write a HDL codes for 2 × 2 bit combinational array multiplier (Both VHDL and verilog). **(08 Marks)**

3 a. Write behavioral description of a half-adder in VHDL and verilog with propagation delay of 10ns. Discuss the important features of their description in VHDL and verilog. **(08 Marks)**

b. Mention the names of sequential statements associated with behavioral description. **(02 Marks)**

c. Write VHDL code for a D latch using variable assignment statement and signal assignment statements. With simulation waveforms clearly distinguish between the two statements. **(10 Marks)**

4 a. Explain with suitable examples, how binding is achieved in VHDL between.
i) Entity and architecture
ii) Entity and component
iii) Library and module. **(06 Marks)**

b. Write a structural description using VHDL to implement a 2:1 multiplexer with active low enable. **(10 Marks)**

c. Explain the use of generate statement. Write down format for it both in VHDL and verilog. **(04 Marks)**

PART – B

5 a. Explain the following syntax with examples: i) Procedure; ii) Task; iii) Function. **(06 Marks)**

b. Write verilog description to convert signed binary to the integer using task. **(08 Marks)**

c. Write a VHDL function to find the greater of two signed numbers. **(06 Marks)**

6 a. Describe procedure for invoking a VHDL entity from a verilog module and a verilog module from a VHDL module. **(08 Marks)**

b. Develop mixed-language description of a 9 bit adder. **(08 Marks)**

c. Write note on VHDL packages. **(04 Marks)**

7 a. What is the necessity of mixed type description? **(04 Marks)**

b. Describe the development of HDL code for an ALU and write VHDL/verilog code for ALU shown below.

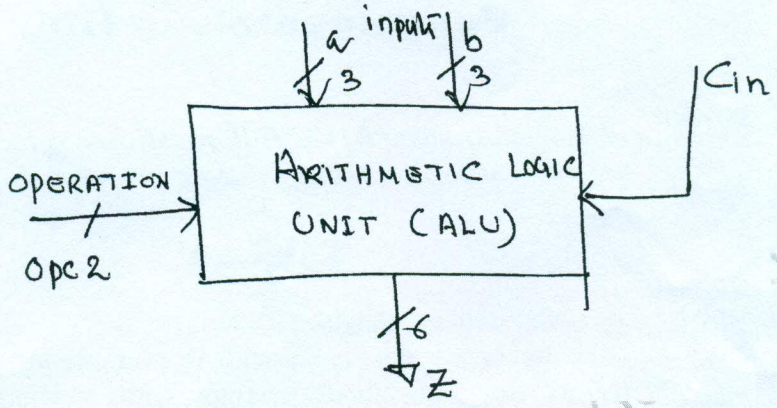

Fig.Q.7(b)

Assume the following operations: Addition, multiplication, division, no operation. **(16 Marks)**

8 a. What is synthesis? List the general steps involved in synthesis. **(08 Marks)**

b. Write VHDL code for signal assignment statement Y = 2* x + 3. Show the synthesized logic symbol and gate level diagram. Write structural code in verilog using gate level diagram. **(12 Marks)**

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