



USN

| | | | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|--|--|
| | | | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|--|--|

10EC45

Fourth Semester B.E. Degree Examination, Dec.2015/Jan.2016

Fundamentals of HDL

Time: 3 hrs.

Max. Marks: 100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART - A

- 1 a. Mention the styles/ types of HDL Description. Explain any 2 types with an example of half adder in both VHDL and verilog. (10 Marks)
- b. Mention the Data types used in VHDL and verilog. (04 Marks)
- c. Distinguish between Verilog and VHDL. (06 Marks)
- 2 a. Write a dataflow description for 4bit ripple carry adder in VHDL and verilog. (10 Marks)
- b. Explain the signal declaration and variable assignment statement used in HDL with an example. (06 Marks)
- c. What are vector data types? Explain them in VHDL and verilog. (04 Marks)
- 3 a. Write behavioral description of 2 : 1 multiplexor using if-else in VHDL and verilog. (08 Marks)
- b. Write behavioral description of half addressing VHDL. (04 Marks)
- c. Write VHDL and verilog codes for 4 x 4 bit Booth algorithms. (08 Marks)
- 4 a. With Logic diagram, write structural description for 2 x 4 decoder with 3 state output both in VHDL and verilog. (10 Marks)
- b. Mention different types of binding. Discuss binding between
 - i) 2 modules in verilog
 - ii) between library and component in VHDL. (10 Marks)

PART - B

- 5 a. Write VHDL description of an N - bit - ripple carry adder using procedures and verilog description using tasks. (10 Marks)
- b. Write verilog function to find greater of 2 signed numbers. (05 Marks)
- c. Write a note on VHDL file processing (05 Marks)
- 6 a. With a block diagram and function table of SRAM, write HDL codes for 16 x 8 SRAM. (12 Marks)
- b. Write a VHDL code for addition of two 5 x 5 matrices, using a package. (08 Marks)
- 7 a. How do you invoke VHDL entity from verilog module? Explain with an example. (08 Marks)
- b. With the help of block dia explain mixed language description of 9 bit adder. (12 Marks)
- 8 a. What is meant by synthesis? List and explain the steps involved in synthesis. (08 Marks)
- b. Design gate level synthesis and write VHDL description for the information given below

| Input | | Outputs |
|-------------|-------|---------------------|
| a | b | z |
| 00 (cent) | 0 - 7 | z = temperature |
| 01 (offset) | 0 - 7 | z = temperature + 4 |
| 10 (half) | 0 - 7 | z = temperature / 2 |
| 11 | xx | z = 15 |
| xx | > 7 | z = 15 |

(12 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8 = 50, will be treated as malpractice.