CBCS SCHEME

USN | | | | | | | | | | | **18EC33**

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain classification of semiconductor insulator and metals using energy band diagram. **(08 Marks)**

b. Explain different types of bonding forces in solids. **(04 Marks)**

c. What are intrinsic and extrinsic materials? Explain briefly by taking suitable example. **(08 Marks)**

OR

2 a. Define Hall effect in semiconductor. Obtain an expression for mobility interms of Hall coefficient and resistivity. **(08 Marks)**

b. Consider a semiconductor bar with width w = 0.1 mm, thickness t = 10 μm, length L = 5 mm. For B = 10 KG (1 KG = 10^{-5} wb/cm^2) and current of 1 mA. We have V_{AB} = −2mV and V_{CD} = 100 mV. Find the type, concentration and mobility of the majority carrier. [Refer Fig.Q2(b)]

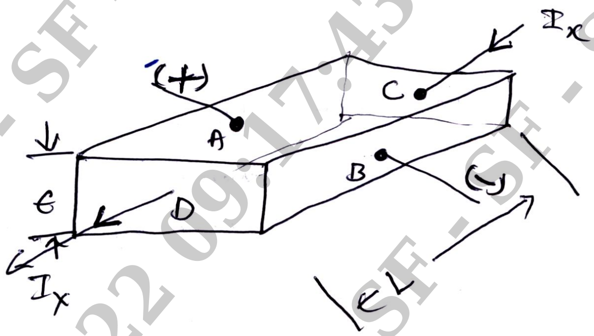

Fig.Q2(b) **(04 Marks)**

c. Derive an expression for conductivity and mobility from random thermal motion or electron in solid. **(08 Marks)**

Module-2

3 a. Explain the reverse bias p-n junction indicating the minority carrier distribution and variation of quasi fermi levels. **(10 Marks)**

b. With a neat diagram, explain in detail Avalanche Breakdown and derive an approximate analysis of avalanche multiplication. **(10 Marks)**

OR

4 a. Derive an expression for current and voltage for an illuminated junction of protodiode and discuss the operation in various quadrants in I-V characteristic. **(08 Marks)**

b. Explain the structure and operation of solar cell. Indicate the significance of Fill Factor. **(08 Marks)**

c. A solar cell has a short circuit current of 100 mA and open circuit voltage of 0.8 V under full solar illumination fill factor is 0.7. What is maximum power delivered to load by this cell? **(04 Marks)**

Module-3

5 a. Explain the summary of hole flow and electron flow in p-n-p transistor with proper biasing and list three dominant mechanism which accounts for I_B. **(10 Marks)**

b. Explain the process flow for double polysilicon self aligned BJT Fabrication. **(10 Marks)**

OR

6 a. Derive Eber's moll modes for Assymetric Transistor (coupled diode model). **(10 Marks)**

b. Write short notes on: (i) Base narrowing (ii) Avalanche Breakdown in transistor **(10 Marks)**

Module-4

7 a. Explain the structure and operation of pn JFET by varying V_{GS} and VDS independently. **(06 Marks)**

b. Write the small signal equivalent circuit of JFET and obtain the expression for transconductance (gm) and plot the graph with respect to V_{gs}. **(06 Marks)**

c. Explain the operation of MOS capacitor using energy band diagram for p-type substrate when:
(i) Negative gate bias
(ii) Moderate positive gate bias
(iii) Large positive gate bias **(08 Marks)**

OR

8 a. Explain the ideal capacitance voltage characteristics of an MOS capacitor with p-type substrate. **(08 Marks)**

b. Explain the operation of n-channel enhancement MOSFET and obtain the current voltage relationship. **(08 Marks)**

c. Write the different types of MOS structures and symbols for each. **(04 Marks)**

Module-5

9 Explain briefly the various steps involved in the fabrication of p-n junction:

a. Rapid thermal processing **(05 Marks)**

b. Ion implementation **(05 Marks)**

c. Chemical Vapor Deposition (CVD) **(05 Marks)**

d. Photolithography **(05 Marks)**

OR

10 a. Write a note on Integrated Circuit (IC) and its advantages and types of ICs. **(10 Marks)**

b. Explain the fabrication of CMOS twin well process. **(10 Marks)**

* * * * *