CBCS SCHEME

USN | | | | | | | | | | 15EC33

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define combinational logic. Design a combinational circuit which takes two, 2 bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is even. **(10 Marks)**

b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates. $D = f(w, x, y, z) = \Sigma m(0, 2, 4, 6, 8) + \Sigma d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

OR

2 a. Define canonical SOP and canonical POS. Expand $f = (\bar{a} + b + c)(a + c + \bar{d})$ into canonical POS. **(04 Marks)**

b. Solve using Quine-McCluskey tabulation method,
$f(a, b, c, d) = \Sigma m(0, 1, 4, 5, 9, 10, 12, 14, 15) + \Sigma\phi(2, 8, 13)$
Obtain the minimal form of the given function. Verify the result using k–map. **(12 Marks)**

Module-2

3 a. Define decoder. Implement full subtractor using a decodes. Write the truth table. **(08 Marks)**

b. Compare ripple carry adder and look ahead carry adder. Explain the circuit and operation of a 4 bit binary adder with look ahead carry. **(08 Marks)**

OR

4 a. Design and implement one bit comparator. **(04 Marks)**

b. Implement the multiple functions :
$f_1(a, b, c, d) = \Sigma(0, 4, 8, 10, 14, 15)$ and
$f_2(a, b, c, d) = \Sigma(3, 7, 9, 13)$
using two 3 to 8 decoders, i.e. 74138 ICs. **(06 Marks)**

c. Implement full adder circuit using 8 : 1 multiplexer. **(06 Marks)**

Module-3

5 a. What is gated SR Latch? Explain the operation of gated SR Latch, with a logic diagram, truth table and logic symbol. **(08 Marks)**

b. Derive the characteristic equation of SR, JK, D and T flip-flops with the help of function tables. **(08 Marks)**

OR

6 a. Explain the operation of a switch debouncer built using SR Latch. Draw the supporting waveforms. **(04 Marks)**

b. Explain 0s and 1s catching problem of Master Slave JK flip flop with waveform. Suggest the solution for this problem. **(04 Marks)**

c. What is edge triggered flip flop? With a neat circuit diagram, explain the operation of positive edge triggered D flip flop, using NAND gates. **(08 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

7 a. With the help of neat diagram, explain PISO and PIPO operation of unidirectional shift registers. **(08 Marks)**

b. Design a 4 bit binary ripple 'UP' counter using negative edge triggered JK flip flop. Show the up counter execution with the help of timing diagram. **(08 Marks)**

OR

8 a. Implement a Mod 8 twisted ring counter using D flip flops. Give the counting sequence and decoding gate inputs. **(06 Marks)**

b. Design a synchronous MOD-6 counter using JK flip flop for the following count sequence 0, 2, 3, 6, 5, 1 and repeat. Write the transition table, logic equations and the counter implementation diagram. **(10 Marks)**

Module-5

9 a. Compare Mealy and Moore sequential circuit models with suitable example. **(04 Marks)**

b. For the logic diagram shown in Fig.Q9(b), write the state and output equations. Give the transition table and the state diagram. **(12 Marks)**

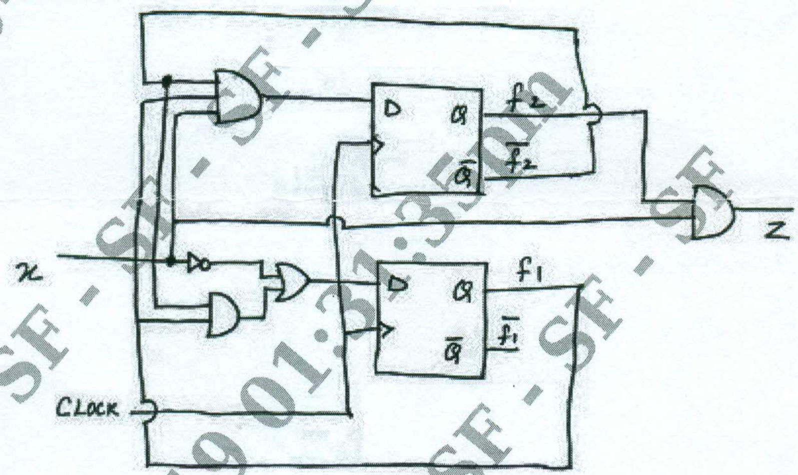

Fig.Q9(b)

OR

10 a. Write the basic recommended steps for the design of a clocked synchronous sequential circuit. **(06 Marks)**

b. How to convert a Mealy machine to a Moore machine? **(02 Marks)**

c. A sequential circuit has one input and one output. The state diagram is shown in Fig.Q10(c). Design a sequential circuit using D flip flop. **(08 Marks)**

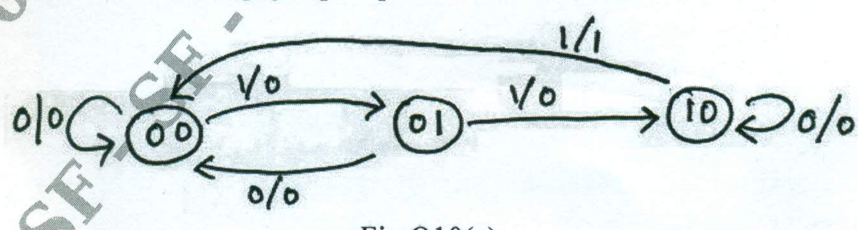

Fig.Q10(c)

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