

# CBCS Scheme



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## Third Semester B.E. Degree Examination, Dec.2017/Jan.2018 Digital Electronics

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

### Module-1

- 1 a. Identify all prime implicants and essential prime implicants of following function using k-map.  
 $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d.c(1, 4, 5, 11, 15)$   
 $f(a, b, c, d) = \pi m(1, 2, 3, 4, 9, 10) + d.c(0, 14, 15)$  (08 Marks)
- b. Find minimal sum for following Boolean function using Quine-McClusky method:  
 $f(a, b, c, d) = \sum m(7, 9, 12, 13, 14, 15) + d.c(4, 11)$ . (08 Marks)

OR

- 2 a. Transform each of following canonical expression into other canonical form in decimal notation.  
 $f(x, y, z) = \sum m(0, 1, 3, 4, 6, 7)$   
 $f(w, x, y, z) = \pi M(0, 1, 2, 3, 4, 6, 12)$  (04 Marks)
- b. Find a minimal sum for following Boolean function using decimal QM method and PI table reduction.  
 $f(a, b, c, d) = \sum m(1, 3, 6, 8, 9, 10, 12, 14) + d.c(7, 13)$ . (12 Marks)

### Module-2

- 3 a. Implement following functions using single 3:8 decoder  
 $f_1(a, b, c) = \pi M(2, 3, 4, 5, 7)$   
 $f_2(a, b, c) = \sum m(1, 3, 5)$ . (04 Marks)
- b. What is magnitude comparator? Design a two bit digital comparator by writing TT, relevant expression and logic diagram. (12 Marks)

OR

- 4 a. Implement  $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 10, 15)$  using  
i) 8:1 MUX with a, b, c as select lines  
ii) 4:1 MUX with a, b as select lines. (08 Marks)
- b. What are the problems associated with basic encoder? Explain how can these problems be overcome by priority encoder considering 8 input lines. (08 Marks)

### Module-3

- 5 a. What is flip-flop. Discuss working principle of SR flip-flop with its TT. Also highlight role of SR f/f in switch debouncer circuit. (08 Marks)
- b. What is significance of edge triggering? Explain working of +ve edge triggered D flip-flop with their functional table. (08 Marks)





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OR

- 6 a. Explain the working of M/S JK flip-flop with functional table and timing diagram. Show how race condition is overcome. (10 Marks)
- b. Obtain characteristic equation for following flip-flops. i) JK ii) SR. (06 Marks)

**Module-4**

- 7 a. Realize a 3 bit binary synchronous up counter using JK flip-flop. Write excitation table, transition table and logic diagram. (10 Marks)
- b. Explain SIPO and PISO shift registers with relevant logic diagrams. (06 Marks)

OR

- 8 a. Explain the working principle of 4bit binary ripple counter configured using +ve edge triggered T – F/F. Also draw timing diagram. (08 Marks)
- b. Explain the operation of universal shift register with a neat diagram. (08 Marks)

**Module-5**

- 9 a. Distinguish between Moore and Mealy model with necessary block diagram. (06 Marks)
- b. Construct mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagram for each state. (10 Marks)

OR

- 10 a. Design a cyclic mod 8 synchronous binary counter using JK flip-flop. Give state diagram, transition table and excitation table. (08 Marks)
- b. Analyse the following sequential circuit shown in figure and obtain :
- i) Flip-flop input and output equation
  - ii) Transition equation (ch.equ)
  - iii) Transition table
  - iv) State table
  - v) Draw state diagram. (08 Marks)

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