10ES33

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Logic Design

Time: 3 hrs.   Max. Marks:100

**Note: *Answer any FIVE full questions, selecting*
*atleast TWO questions from each part.***

PART – A

1 a. A logic circuit has 4 inputs P, Q, R, S and 2 outputs Y_1, Y_2.
   i) Y_1 is '1' when majority of inputs are '1' (equal numbers of '0' and '1' are treated don't care)
   ii) Y_2 is '1' when two adjacent inputs are '1' (P and S are treated adjacent)
   Design the circuit using NAND gates only.   **(12 Marks)**
   b. Determine minimal POS and SOP for $f(E, F, G, H) = \pi (0, 1, 2, 7, 11, 13) \cdot d(4, 5, 8, 10, 14)$.
   (08 Marks)

2 a. Using Quine – McCluskey technique simplify the Boolean expression.
   $f(A, B, C, D) = \Sigma(0, 5, 7, 8, 9, 10, 11, 14, 15)$.   **(10 Marks)**
   b. Simplify and realize the given function using MEV technique taking lest significant variable as map entered variable.
   $f(a, b, c, d, e) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25\ 27, 28, 30)$. **(10 Marks)**

3 a. With the help of logic diagram, truth table and circuit diagram, explain 3–to–8 line decoder with active low outputs. Using the same implement the functions :
   $f_1 = \pi(0, 3, 5, 6)$
   $f_2 = \pi(2, 3, 4, 5, 7)$.   **(10 Marks)**
   b. What are the limitations of basic encoder? Design a 4–2 priority encoder with validity output.   **(10 Marks)**

4 a. Explain how look Ahead carry adder speeds up operation of addition over basic parallel adder.   **(10 Marks)**
   b. Implement $f(A, B, C, D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$ using i) 74151 (8–1 MUX) ii) 74153 (dual 4–1 mux).   **(06 Marks)**
   c. Define Dmux, design 1–4 Dmux.   **(04 Marks)**

PART – B

5 a. Explain the application of SR Latch as switch de-bouncer.   **(06 Marks)**
   b. Explain the operation of asynchronous inputs of flip-flop with waveforms. **(06 Marks)**
   c. Write the logic circuit and truth table of D and T FFS. Draw the output waveforms for the input shown for :
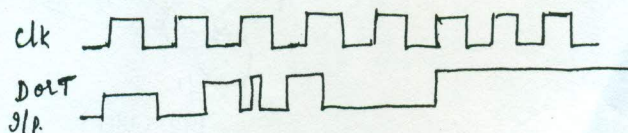   i) D latch   ii) Gated D latch   iii) +ve edge TFF   iv) –ve edge TFF. **(08 Marks)**

Fig. Q5(c)

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6 a. Design a mod16 asynchronous down counter using D flip–flops. **(10 Marks)**
   b. Explain the operation of : i) parallel in serial out shift register   ii) twisted ring counter. **(10 Marks)**

7 a. Differentiate between Moore and Mealy models. **(05 Marks)**
   b. Construct the transition table, state table and state diagram for the Moore sequential circuit shown. **(15 Marks)**
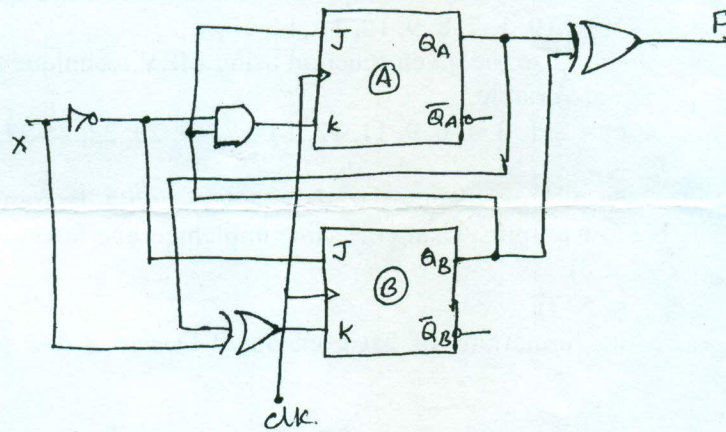

Fig. Q7(b)

8 a. Explain lockout condition. How do you eliminate it? Design a synchronous counter for :
       $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4$.
       Avoid lockout condition. Use JK flip-flop. **(12 Marks)**
   b. A sequential circuit has one input and one output. The state diagram is as shown in Fig. Q8(b). Design the circuit using D FF. **(08 Marks)**
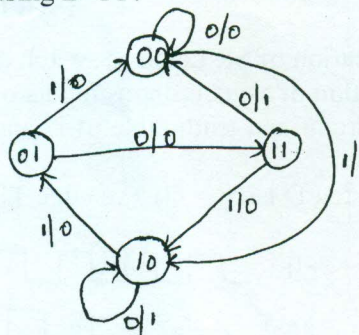

Fig. Q8(b)

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