USN | | | | | | | | | | |

10ES33

Third Semester B.E. Degree Examination, Dec.2015/Jan.2016
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define combinational logic. Two motors M_2 and M_1 are controlled by three sensors S_1, S_2 and S_3. One motor M_2 is to run any time when all three sensors are on. The other motor (M_1) is to run whenever sensors S_2 or S_1 but not both are on and S_3 is off. For all sensors combinations where M_1 is on, M_2 is to be off, except when all sensors are off and then both motors remain off. Construct the truth table and write the Boolean output equation. **(05 Marks)**

b. The following Boolean function into their proper canonical form in decimal notation.
i) $M = p(q' + s)$
ii) $N = (w' + x)(y + z)$ **(07 Marks)**

c. Reduce the following Boolean function using K-map and realize the simplified expression using NAND gates.
$T = f(a,b,c,d) = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$ **(08 Marks)**

2 a. Simplify the following function using Quine-McClusky method and realize the simplified using NOR gates.
$P = f(w,x,y,z) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$ **(12 Marks)**

b. Simplify $f(a,b,c,d) = \sum m(0,4,5,6,13,14,15) + \sum d(2,7,8,9)$ using MEV technique using basic gates. **(08 Marks)**

3 a. Design a combinational circuit to find the 9's complement of a single digit BCD number. Realize the circuit using suitable logic gates. **(08 Marks)**

b. Draw the logic diagram for 2 to 4 line decoder with an active low encoder enable and active high data output. Construct a truth table and describe the circuit function with logic symbol (74139IC's) for the decoder. **(06 Marks)**

c. Design a 4 to 16 line decoder using 2 to 4 line decoder which has the active low outputs and active low enable input. Explain its operation. **(06 Marks)**

4 a. Design a binary full adder using only two input NAND gates. Write a truth table. **(06 Marks)**

b. Implement the following Boolean function using 4 : 1 multiplexer (MUX)
$Y = f(A,B,C,D) = \sum m(0,1,2,4,6,9,12,14)$ **(06 Marks)**

c. Define magnitude comparator. Design a two-bit binary comparator and implement with suitable logic gates. **(08 Marks)**

PART – B

5 a. Discuss the difference between a flip flop and latch. Explain the operation of gated SR latch with a logic diagram, truth table and logic symbol. **(06 Marks)**

b. Explain the working of Master Slave JK flip flops with functional table and timing diagram. Show how race around condition is overcome. **(08 Marks)**

c. Obtain the characteristic equation of JK and SR flipflops. **(06 Marks)**

6 a. Describe the block diagram of a MOD-'n' twisted ring counter and explain its operation with the count sequence table and decoding logic used to identify the various states. **(08 Marks)**

b. Design a mod-6 synchronous counter using clocked JK flipflops, the count sequence being 0, 2, 3, 6, 5, 1, 0, 2……. **(12 Marks)**

7 a. With a suitable block diagram, explain the Mealy and Moore model, in a sequential circuit analysis. **(10 Marks)**

b. Explain 4 bit universal shift Register using 4 : 1 MUX with help of logic diagram. Write a mode control table. **(10 Marks)**

8 a. Describe the following terms with respect to sequential machines:
i) State ii) Present states iii) Next states. **(06 Marks)**

b. A sequential circuit has one input one output. The state diagram is shown in Fig. Q8 (b). Design a sequential circuit with T flip flops. **(14 Marks)**

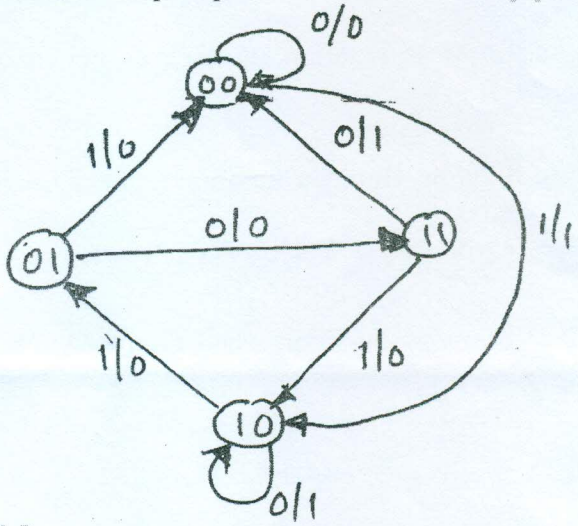

Fig. Q8 (b)

* * * * *