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10ES32

Third Semester B.E. Degree Examination, June/July 2015
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. State and explain the various resistance levels of the semiconductor diode. **(06 Marks)**

b. Explain the working of a full wave centre tapped rectifier. Also determine ripple factor, efficiency and voltage regulation. **(10 Marks)**

c. Design a suitable circuit represented by the box shown below, which has the input and output waveforms as indicated. **(04 Marks)**

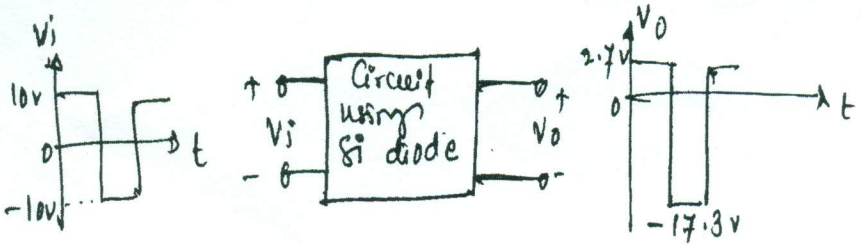

Fig. Q1(c)

2 a. Name different biasing methods of transistor. With circuit diagram analyze the fixed bias circuit, with effect of variation in I_B, R_c and V_{CC} on Q. point of the load line. **(10 Marks)**

b. Explain the circuit of a transistor switch being used as an inverter. **(04 Marks)**

c. In a voltage divider bias circuit of BJT. V_{CC} = 20 V, R_C = 10 kΩ, RE = 1.5 kΩ, R_1 = 40 kΩ, R_2 = 4 kΩ. Assume silicon transistor with β = 150. Find I_C, V_{CE} and $I_{C(sat)}$ using exact analysis. **(06 Marks)**

3 a. Define h – parameters and hence derive h – parameters model of CE – BIT. **(06 Marks)**

b. Explain with a neat circuit diagram of emitter follower configuration. Justify how voltage gain is nearly equal to one. **(06 Marks)**

c. For the circuit shown below determine V_{CC}, if A_V = –160 and r_0 = 100 kΩ. Take β = 100. **(08 Marks)**

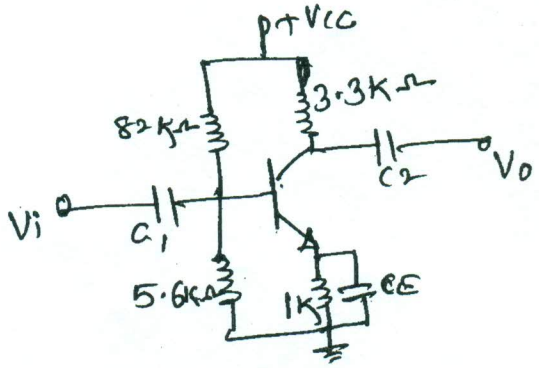

Fig. Q3(c)

4 a. Draw the single stage RC coupled BJT amplifier and discuss the effect of (low frequency response) : i) Input capacitance C_S ii) output capacitance C_C and iii) Emitter by pass capacitance C_e on frequency response. **(05 Marks)**

b. Prove that miller effect of input capacitance $C_{Mi} = (1 - A_v) Cf$ and output capacitance $C_{M0} = \left(1 - \frac{1}{A_v}\right) C_f$. **(10 Marks)**

c. It is desired that the voltage gain of an RC – coupled amplifier at 60 Hz should not decrease by more than 10% from its mid bond value. Calculate :
i) the lower 3 dB frequency
ii) the required C if R = 2000 Ω. **(05 Marks)**

PART – B

5 a. Derive expressions for Z_i and A_i for a Darlington emitter follower circuit. **(10 Marks)**

b. Mention the types of feedback connections. Draw their block diagrams indicating input and output signal. **(06 Marks)**

c. List the general characteristics of a negative feedback amplifier and write its advantages. **(04 Marks)**

6 a. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier. **(07 Marks)**

b. Explain the operation of a class B push-pull amplifier and derive its conversion efficiency. **(08 Marks)**

c. The following distortion reading are available for a power amplifier :
$D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$, with $I_1 = 3.3$A and $R_C = 4\ \Omega$. Calculate :
i) the THD ii) the fundamental power component iii) the total power. **(05 Marks)**

7 a. Explain the working of Wien bridge oscillator. **(07 Marks)**

b. With a neat circuit diagram, explain the operation of BJT Colpitts oscillator. **(06 Marks)**

c. A crystal has the following parameter L = 0.334 H, C_M = 1 pF, C = 0.065 and R = 5.5 kΩ. Calculate the series resonant frequency, parallel resonant frequency and find Q of the crystal. **(07 Marks)**

8 a. Draw the JFET common drain configuration (source – follower) circuit. Derive Zi, Z_0 and A_v using small signal model. Write its characteristics. **(10 Marks)**

b. Compare JFET and MOSFET. **(03 Marks)**

c. For the JFET common drain configuration shown below. Given I_{dss} = 10 mA, V_P = –5V, r_d = 40 kΩ, V_{GSQ} = –2.85 V i) Calculate Z_i and Z_0 ii) Calculate A_v iii) find V_0 if V_i = 20 mV (p – p). **(07 Marks)**

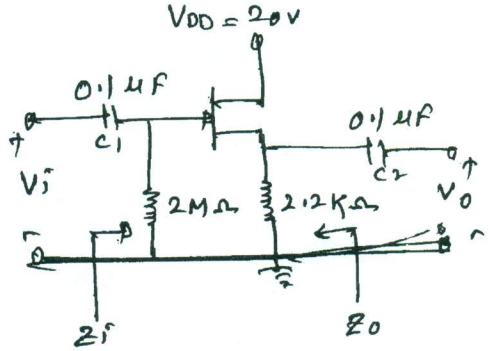

Fig. Q8(c)

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