Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Advanced Computer Architecture

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a. With a neat diagram explain the elements of modern computer system.   (08 Marks)
    b. Explain Flynn's classification of computer architecture.   (08 Marks)

OR

2   a. Define data dependency. Explain different functions of data dependency with the help of dependency graph.   (08 Marks)
    b. A 4 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts.

Instruction type	Instruction count	Cycles/instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program.   (08 Marks)

Module-2

3   a. Explain the architecture of VLIW processor and its pipeline operations.   (08 Marks)
    b. Explain the inclusion property and locality of reference along with its types in multilevel memory hierarchy.   (08 Marks)

OR

4   a. Explain page replacement policies with the help of an example.   (08 Marks)
    b. Give the characteristics of symbolic processors.   (08 Marks)

Module-3

5   a. Explain bus arbitration and its types in multiprocessor systems.   (08 Marks)
    b. Explain any two mapping techniques.   (08 Marks)

OR

6   a. Explain the following terms associated with cache and memory architecture:
        (i) Low order memory interleaving
        (ii) Atomic v/s non-atomic memory
        (iii) Physical address cache vs virtual address cache
        (iv) Memory bandwidth and fault tolerance.   (08 Marks)

b. Consider the following pipelined processor within 3 stages this pipeline has total evaluation time of 8 clock cycles. All successor stages must be used after each clock cycle.

	0	1	2	3	4	5	6	7	8
S_1	X								X
S_2		X	X					X	
S_3				X					
S_4					X	X			
S_5							X	X	

(i) List the set of forbidden latencies between task initiations
(ii) Draw the state diagram which shows all possible latency cycles
(iii) List all greedy cycles
(iv) Value of MAL. **(08 Marks)**

Module-4

7 a. Explain hierarchical bus system with neat diagram. **(08 Marks)**
   b. Explain crossbar networks along with its advantages and limitations. **(08 Marks)**

OR

8 a. Explain snoopy protocols with its approaches. **(08 Marks)**
   b. Briefly explain message routing schemes. **(08 Marks)**

Module-5

9 a. Define parallel programming model. Explain any two models. **(08 Marks)**
   b. Mention branch prediction methods and explain. **(08 Marks)**

OR

10 a. With the help of a neat diagram explain compilation phases in code generator. **(08 Marks)**
    b. Explain different language features for parallelism. **(08 Marks)**

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