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Dr. Mohandas Bhat S.

It gives me immense pleasure to bring into your information that Sahyadri released the third volume of JSR journal and thanks to all the contributors for making it a very success.

Research is a passion. It is an integral part of engineering profession of 21st century. Research is for the benefit of public for making the life safe and better. To get the benefits of research the results should be shared with other researchers and users. Journals are the media for sharing the researchers' inventions and innovations with all stake holders.

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Yours

Developments in 2.5D: The Role of Silicon Interposers

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Silicon interposers are a technology with a history of multiple incarnations over more than 20 years. Today, interposers with TSVs are considered an alternative to 3D IC structures where die are stacked on top of each other using TSVs. Applications for interposers with TSVs include ASICs for networking applications and FPGAs. Xilinx's Virtex-7 2000T FPGA was one of the first new products using a silicon interposer with TSVs for a partitioned IC design. Co-design with new packaging technology has resulted in a new FPGA that allows reduced system cost and increased performance with lower power. By not having to drive off-chip I/Os across PCB traces to adjacent FPGAs, high-performance applications that have previously used multiple FPGAs can be replaced with a single package solution that provides high-bandwidth, low-latency, power-efficient interconnect between the FPGA die. The key to the performance gains is the partitioning of an FPGA die into four “slices” that are mounted on a silicon interposer. Is this a unique application or are there other potential applications for interposers in applications with GPUs or ASICs? Today's interposers are passive structures, but there are potential for the use of integrated passives in the interposer. How do these applications differ from the technology introduced in previous generations? This presentation highlights the new drivers for the introduction of silicon interposers. The presentation also examines the latest developments in the infrastructure to support the development of this technology, including suppliers. The article also highlights the differences between adoption of today's interposers and the thin-film on silicon (MCM-D) of the past.

Advantages of Silicon Interposers

With the need for higher performance and smaller form factors, many companies are embracing the use of silicon interposers with through silicon vias (TSVs). The drivers are mainly partitioning large die, integrating single chips into a module, reducing die size where substrate density is the constraint, and the use of the interposer to minimize the stress on large die with extra-low-k (ELK) dielectrics.

The advantages of silicon interposers result from the combination of the silicon material properties and multichip packaging.

Advantages include:

- High wiring density
- TCE matched to the silicon die that can reduce the chip-to-package interaction especially with extra-low-k (ELK) dielectrics
- Excellent electrical and thermal performance
- Lower cost of active devices due to partitioning large die
- Lower power requirements than equivalent single-chip packages due to multiple chips combined on one substrate
- Possibility of integrating passives into the substrate

History Lessons from MCM Days

AT&T and IBM's work with silicon interposer dates back to the late 1980s. Throughout the 1990s silicon multichip module (MCM) work was underway at various companies. Thin-film-on-silicon MCM-D where the D stood for "deposited" was one substrate choice competing with laminate (MCM-L) and ceramic (MCM-C) substrates. The benefits of silicon include a denser, higher-performance module than laminate substrate offered. Ultimately, the technology did not penetrate the high-volume commercial market and lost the battle to laminates because of cost and logistics. The competing laminate substrates were less dense but had much lower cost. From a logistics standpoint, the higher density of the silicon substrate could not be fully utilized because the large number of high lead-count die that it could support created a package that was extremely difficult to test and had low yields. Know good die was a critical issue in assembly and final yield [1]. A technology that could not find a market in 1995 is generating a different response today because packaging and integration have evolved substantially, but the ghost of the MCM-D past is still there and issues of substrate cost, KGD, test, infrastructure and logistics, and final yield must be addressed.

New Applications for Silicon Interposers

Silicon interposers are used as LED sub-mounts and in RF applications where integrated passives are found in the dielectric layer. These applications are not necessarily fine geometry interposers and do not contain through silicon vias (TSVs), but are in production. IPDiA supplies interposer for sub-mounts and also manufacturer's silicon interposer for RF modules. STATS ChipPAC supplies silicon interposers with integrated passives for RF module applications [2]. Several companies use silicon interposer with backside vias for MEMS applications. IBM supplies a silicon interposer with TSVs to Semtech Corporation for a mixed signal application. Applications include receivers for fiber optic telecommunications, high-performance RF, test equipment and instrumentation, and phased array radar systems. A number of companies and research institutes are discussing the use of silicon interposers in photonics applications.

Recently announced applications for silicon interposers are focused on high-performance applications such as network systems, servers, and graphics. Devices currently under consideration for use with fine feature interposers include graphics processors, CPUs, and high-end ASICs. Table 1 shows potential applications, and the estimated adoption timeline.

Application	HVM Start	Barrier
FPGAs	end of 2011/2012	None
Tablets	2015?	Cost Supplier availability
Graphics Processors	2015-2016	Immature infrastructure Silicon interposer cost
Networking	2015-2017	Immature infrastructure No roadmap for larger interposers
Server	2016	Cost Reliability
Automotive	2018?	Cost Reliability

Table 1. Interposer Adoption Timeline and Barriers
Source:TechSearch International, Inc.

Xilinx has introduced four products in its Virtex FPGA family that use silicon interposers (see Figure 1). The devices are 28nm homogeneous and heterogeneous modules using silicon interposers. The first product, a homogeneous part with four “slices” mounted on a passive interposers containing TSVs started shipping at the end of 2011. The Virtex HT parts are heterogeneous modules combining FPGA "slices" with 28Gbps mixed signal transceiver die. These parts offer the largest single-FPGA solution for 100G to 400G line cards for next-generation communication systems [3]. One of the key benefits of physically separating the digital FPGA from the transceivers is noise isolation. This ensures the lowest possible jitter and noise to simplify design closure and reduce board cost. Implementing the analog transceivers on separate devices also reduces design complexity and optimizes performance of both the digital and analog components. The heterogeneous architecture also allows Xilinx to provide up to sixteen 28G transceivers, enabling extremely high bandwidth. The Virtex-7 H580T began production in May 2012. Xilinx's interposers are manufactured by TSMC, using the (CoW)oS process. In this process, the dies are assembled to the interposer while it is still in wafer form.

Thin silicon interposers are targeted for use in high-end GPUs. High-bandwidth memory has a 40µm bump pitch, so a dense substrate is required to route out the bumps. Network system makers such as Cisco have roadmaps that show the adoption of silicon interposers. ASIC suppliers have plans to provide silicon interposer solutions to meet these requirements.

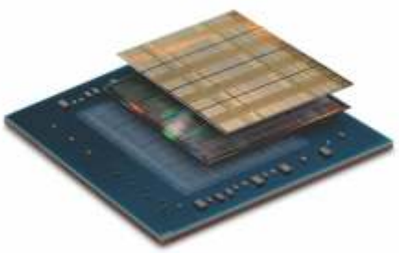

Figure 1:
Xilinx “Stacked Silicon Interconnect” (2.5D)

For many applications, including network systems, stacked memory that can be mounted on the interposer next to the logic device is required and adoption depends on the availability of stacked memory from key memory suppliers. Micron has announced shipments of engineering samples of its Hyper Memory Cube (HMC) that is packaged in a BGA. While there is collaboration with Altera on a network systems solution using Altera's FPBGAs, the current version of the HMC would not be mounted on a silicon interposer. Stacked memory from other suppliers is an anticipated for several applications, but timing is still unclear.

Companies such as nVIDIA note that barriers include immature infrastructure and the lack of availability of a cost-effective silicon interposer. According to Altera, micro-bump stacking is the most critical challenge in 2.5D package assembly. It is affected by warpage, and is more problematic for large parts like interposers [4].

Suppliers of Interposers

TSMC has been main supplier of fine feature size silicon interposers, but other suppliers are coming on line and production is scheduled to ramp. Current and potential silicon interposer suppliers include ALLVIA, ASE, Dai Nippon Printing, GLOBALFOUNDRIES, Ibiden, IBM, IMT, IPDiA, NEPES, Shinko Electric, Silex Microsystems, SPIL, STATS ChipPAC, Tezzaron and its Novati subsidiary, TSMC, and UMC.

Cost, Cost, Cost

The cost of the interposer is a concern for some applications and alternatives such as organic or glass interposers are being examined. Historically, much of the cost in silicon interposer fabrication was in via fabrication and fill. Throughputs for via etch and fill have improved. SavanSys Solutions has developed cost models to examine both 3D and 2.5D solutions and the company reports that much of today's cost is associated with yield. For example, low assembly yield at the micro bump joining can result in scrapped interposers and contributes to the total cost. Via formation and fill throughputs have improved, as has via reveal and these process costs are reported to be lower than RDL process costs.

Conclusions

Today's applications for silicon interposers are primarily MEM's and FPGA's. There are potential applications for silicon interposers in ASIC, CPU for server, GPU and wireless devices using integrated passive applications. There still are major concerns about suppliers and assembly capability. It is expected that there will be a need for new players and business models prior to full adoption. While 3D technologies show high potential, there are still issues with TSV technologies that need to be addressed. There is still a lot of work to be done in this area of development. In the near term, 2.5D technologies will have to fill the gap. Finally, cost is one of the biggest barriers to adoption and alternative materials to silicon are being explored by research organizations around the world, such as glass panels.

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Electrical Characterization of MFeOS Gate Stacks for Ferroelectric FETs

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We have investigated the electrical characterization of Metal-Ferroelectric-Oxide-Semiconductor (MFeOS) structure for non volatile memory application. Al/PZT/Si and Al/PZT/SiO_2/Si capacitors have been fabricated using PZT (35/65) as the ferroelectric layer. The maximum C-V memory window of 6 V for Metal-Ferroelectric-Semiconductor (MFeS) structure and 2.95 V and 6.25 V for MFeOS capacitors having 2.5 nm and 5 nm buffer layer respectively was obtained. Our comparative data shows higher dielectric strength and lower leakage characteristic for MFeOS structure having 5 nm SiO_2 buffer layer as compared to MFeS structure. Also leakage characteristic was observed to be considerably influenced by annealing conditions.

"Electrical Characterization of MFeOS Gate Stacks for Ferroelectric FETs," Materials Science in Semiconductor Processing, Elsevier, Vol.16, pp.1603–1607, 2013.

Online Available: http://www.journals.elsevier.com/materials-science-in-semiconductor-processing/recent-articles/

Receiver Based Multicasting Protocol for Wireless Sensor Networks

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Multicasting is purely based on the creation and maintenance of structures called tree or mesh for routing of packets. Each individual node has to maintain state information about these structures. In wireless sensor networks, the maintenance of this information leads control overhead. So that, the new protocol called receiver based multicasting protocol is developed which does not require any state information for routing the packets. The routing depends only on the location information of the multicast members (destinations) and the list of multicast members is added in packet header. This removes maintenance of state information. The Receiver Based Multicasting (RBMulticast) Protocol is implemented in Network Simulator (NS2). The results and performance analysis shows the improvement in packet delivery and less energy consumption.

"Receiver Based Multicasting Protocol for Wireless Sensor Networks," International Journal of Engineering Research and Technology (IJERT), Vol 3, Issue 1, ISSN: 2278-0181, Jan 2014.

Online Available: http://www.ijert.org/view.php?id=7532&title=receiver-based-multicasting-protocol-for-wireless-sensor-networks

Heightening the Data Security and Network Lifetime in Ad Hoc Network

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Ad hoc Networks are defined as the category of wireless networks that utilize multi-hop radio relaying and are capable of operating without central coordinator which makes routing a challenging task. Ad Hoc network routing is the reactive on- demand philosophy where routes are established only when required. Generally, in this type of network the exhaustion of energy will be more and as well, the security is missing due to its infrastructure less nature. Due to the lack of energy, the link failure may occur and the network lifetime also gets affected. Thus these may affects the performance of the network. To overcome these problems, we have proposed a new algorithm. This algorithm holds two mechanisms. Initially, it provides the security against attacks using new cryptographic mechanism. Secondly, routing the packets in the efficient path by checking the residual power in each node. By simulation based studies, we have proved that this algorithm effectively provides higher security and increases the network lifetime.

"Heightening the Data Security and Network Lifetime in Ad Hoc Network," International Journal of Advances in Management Technology and Engineering Sciences (IJAMTES), Vol 2, Issue 8(III), pp. 28-33, ISSN 2249-7455, May 2013

Effect of Nitrogen Containing Plasma on Interface Properties of Sputtered ZrO_2 Thin Films on Silicon

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The present paper deals with the electrical characterization of sputtered ZrO_2/Si interface deposited in N_2 containing plasma. Incorporation of nitrogen in the sputter deposited films was confirmed by glancing angle X-Ray diffraction measurement. MOS C–V and I–V techniques were used for interface characterization. Nitrogen incorporated ZrO_2 MOS capacitors exhibited higher breakdown voltage and lower leakage current than structures having ZrO_2 dielectric films sputtered in pure argon atmosphere. Different device parameters such as flat band voltage, leakage current, breakdown voltage, charge defects were extracted and compared with and without nitrogen incorporated ZrO_2/Si MOS capacitor structures. The effect of post deposition annealing on the electrical behavior of ZrO_2/Si interface was also investigated.

"Effect of Nitrogen Containing Plasma on Interface Properties of Sputtered ZrO2 Thin Films on Silicon," Materials Science in Semiconductor Processing, Elsevier, Vol.19, pp. 145-149, 2014.

Online Available:

http://www.researchgate.net/publication/259522250_Effect_of_nitrogen_containing_plasma_on_interface_properties_of_sputtered_ZrO2_thin_films_on_silicon

Improving the Performance Efficiency of Virtual Machines in Cloud Data Centres using Dynamic consolidation

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Cloud computing is a set of IT services that are provided to a customer over a network on a leased based manner and with the ability to scale up or down their service requirements. Cloud computing model have led to the establishment of large-scale virtualized data centers. Such data centers consume enormous amounts of electrical energy resulting in high operating costs. In addition, high energy consumption by the infrastructure leads to substantial carbon dioxide (CO_2) emissions contributing to the greenhouse effect. By switching the idle node off and by using Dynamic consolidation of virtual machines the Cloud providers can optimize resource usage and reduce energy consumption. Virtualization technologies which are heavily relied on by the Cloud computing environments provide the ability to transfer virtual machines (VM) between the physical systems using the technique of live migration mainly for improving the energy efficiency. Dynamic server consolidation through live migration is an efficient way towards energy conservation in Cloud data centers. The focus of this work is on energy and performance efficient resource management strategies that can be applied in a virtualized data center by a Cloud provider (e.g. Amazon EC^2). Performance characteristics of online algorithms for the problem of energy and performance efficient dynamic VM consolidation are investigated.

"Improving the Performance Efficiency of Virtual Machines in Cloud Data Centres using Dynamic consolidation," International Journal of Advances in Management Technology and Engineering Sciences (IJAMTES), Vol 2, Issue 8(III), pp. 71-75, ISSN 2249-7455,May 2013.

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Splitting of Fundamental Particle Photon - A Break through for Superfast Quantum Computers

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Gone are the days of splitting or dividing atomic or subatomic particles but the physicists have achieved to isolate fundamental particles such as photons i.e., light particle [electromagnetic wave] from their environment without destroying their quantum properties. Then what about the fundamental particle status of the photon particle?

The behaviour of the individual constituents that make up our world – atoms (matter) and photons (light) is described by quantum mechanics. These particles are rarely isolated and usually interact strongly with their environment. The behaviour of an ensemble of particles generally differs from isolated ones and can often be described by classical physics. From the beginning of the field of quantum mechanics, physicists used thought experiments to simplify the situation and to predict single quantum particle behaviour.

Fundamental particles such as photons are difficult to isolate from their environment without destroying many of the mysterious quantum properties that make them interesting for physicists to study. In the 1980s, David J Wineland of the US National Institute of Standards and Technology and the University of Colorado, Boulder and Serge Haroche is a professor at the Collège de France and Ecole Normale Supérieure in Paris independently invented ways to trap particles while maintaining their quantum properties. Wineland used electric fields to trap electrically charged atoms, keeping them away from heat and radiation by conducting his experiments at very low temperatures and in a vacuum. Haroche trapped particles of light between superconducting mirrors that are cooled to a fraction above -273oC, or absolute zero.

The Nobel prize for physics for the year 2012 has been awarded to two scientists who worked out a way to trap, manipulate and study the fundamental particles of light and matter without destroying them. Their work is a crucial step towards building superfast quantum computers and could lead to ways of measuring time with a hundred times greater precision than is possible using atomic clocks. An atomic clock is a clock device that uses an electronic transition frequency in the microwave, optical, or ultraviolet region of the electromagnetic spectrum of atoms as a frequency standard for its timekeeping element. Atomic clocks are the most accurate time and frequency standards known, and are used as primary standards for international time distribution services, to control the wave frequency of television broadcasts, and in global navigation satellite systems such as GPS. In the case of photon division, transition frequency will be more thereby leading to higher accurate measurement of time.

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Quantum Computers

In a theoretical article published in 1995, Cirac and Zoller suggested a way to build a quantum computer with trapped ions. Quantum bits (qubits) are encoded into hyperfine levels of trapped ions, which interact very weakly with the environment and therefore have long lifetimes. Two or more ions can be coupled through the center-of-mass motion. Wineland and his group were the first to carry out experimentally a two-qubit operation (the Controlled NOT gate, CNOT) between motion and spin for Be+ ions Since then, the field of quantum information based on trapped ions has progressed considerably. In 2003, Blatt and collaborators in Innsbruck, Austria, achieved a CNOT operation between two Ca+ ions . Today, the most advanced quantum computer technology is based on trapped ions, and has been demonstrated with up to 14 qubits and a series of gates and protocols. Developing large devices capable of carrying out calculations beyond what is possible with classical computers will require solving substantial challenges in the future.

Optical Clocks

An important application of Wineland's research with trapped ions is optical clocks. Clocks based on a transition in the optical domain are interesting because the frequency of the transition, which is in the visible or ultraviolet range, is several orders of magnitude higher than that of the Cesium clocks operating in the microwave range. Optical clocks developed by Wineland and Coworkers currently reach a precision just below 10-17, two orders of magnitude more accurate than the present frequency standard based on Cs clocks.

An optical ion clock uses a narrow (forbidden) transition in a single ion, insensitive to perturbations. The ion also needs to have strong allowed transitions for efficient cooling and detection. Wineland and colleagues developed a new technique, called quantum logic spectroscopy, based on entanglement of two ion species. In this technique, one ion provides the spectroscopy transition [e.g., 1S0→3P1 in 27Al+ (267 nm)], while the other one (e.g., 9Be+) has the strong cooling transition (Schmidt et al., 2005). The precision of two different optical clocks can be compared with the help of the frequency comb technique invented by Hänsch and Hall (2005 Nobel Prize in Physics).

The accuracy recently achieved by the optical clocks has allowed Wineland and coworkers to measure relativistic effects, such as time dilation at speeds of a few kilometers per hour or the difference in gravitational potential between two points with a height difference of only about 30 cm.

With quatum computers and high precision clock what must be the speed and efficiency of the poor(!) human individual.. . run with the velocity of light! relativistic variations neglected!!!

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Source: Internet

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